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MICROELECTRONIC AND MICROMECHANICAL SENSORS AND ACTUATORS IN CMOS TECHNOLOGY - A NOVEL SCHEME TOWARDS REGULARIZATION AND INTEGRATION

by

MEENAKSHINATHAN PARAMESWARAN

©

A THESIS

SUBMITTED TO THE FACULTY OF GRADUATE STUDIES AND RESEARCH

IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE

DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL ENGINEERING

EDMONTON, ALBERTA

SPRING 1990

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Dedicated

To my wife Kalpagam

ABSTRACT

Present day integrated circuit (IC) as well as sensor technology stem from silicon microelectronic processing with one marked difference in their direction of progress. IC technology is being developed in the direction of commercial accessibility, while the sensor technology still relies upon customization of fabrication techniques and consequently its development is restricted to selected research groups. An attempt has been made to overcome this serious limitation by regularizing the microsensor fabrication scheme using a commercially well-established IC technology. A simple, yet powerful approach has emerged as a result of this attempt. Many inherent features of commercial CMOS technology have been identified and found to be ideally suited for microsensor fabrication. Based on these features, a special sensor layout design procedure has been introduced to achieve complete compatibility with the CMOS technology, without altering any of the CMOS process sequences. Under this scheme, fabrication of sensors and actuators has become possible in just two steps, namely layout design step and a single post-processing step. The approach leads to several advantages. First, the major obstacle for the progress of the sensor development is overcome by eliminating the requirement for customized fabrication facilities. Secondly, a direction has been set forth to regularize the sensor fabrication approach as it exists in today's integrated circuit technology. This implies that sensors and actuators of different kinds are realizable using a fixed technique. Thirdly, realization of integrated sensor systems with on-chip electronics becomes easily feasible since the circuit forming capabilities of the CMOS process remain unaffected in the entire scheme.

Several devices have been successfully fabricated and tested using this scheme. The devices include integrated humidity sensors and micromechanical structures such as bare polysilicon microbridges, sandwiched oxide microbridges, cantilevers and suspended plates. Functional devices such as electro-thermal gas flow sensors, thermal and visible

radiation sources and electro-thermal microactuators have also been realized using the sandwiched oxide micromechanical structures. The on-chip circuit integration capabilities have been demonstrated by various designs and tests. The functioning of the fabricated devices has been studied systematically and the results are reported. A simple analytical scheme has been developed to model the thermally isolated micromechanical structures. Modeling results are compared with various experimental results.

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1. INTRODUCTION

Sensors and actuators of different kinds have assumed an indispensable place in today's science and technology. Their applications range from simple household airconditioning to complex process control for the semiconductor industry. Among them, electronic sensors are very popular and widely used because of their direct interfacibility with computers and other modern electronic systems. With the advent of microelectronic processing technology miniaturization of sensors to the level of micron dimensions became possible. Sensors, in their miniaturized form occupy less space, consume less power and facilitate the production of portable measurement and monitoring systems. Functionally, they are noted for their minimum influence on the measurand, thereby ensuring relatively high accuracy of measurement.

1.1 Microelectronic processing technology

Microelectronic processing technology has been the key factor for the success behind integrated circuit (IC) technology [1, 2]. Its extension to the fabrication of sensors and actuators in recent times has resulted in significant contributions in the field of sensor technology as well [3]. Apart from drastically reduced physical dimensions and low power requirements, batch fabrication of sensors has become possible by using microelectronic processing technology [1, 3]. This feature is extremely important for commercial and scientific purposes because devices as high as hundreds and thousands in number can be fabricated on a single silicon wafer. Also, the price of the sensor element is significantly lowered. Because of these advantages, microelectronic processing remains as a preferred technology for the commercial fabrication of various sensors. The issues related to microelectronic processing equally apply to the case of microelectronic actuators as well.

1.2 Support electronics

Regarding microelectronic sensors and actuators, emphasis is placed on the *support electronics* which are absolutely essential for their functioning [4]. Circuit elements such as current mirrors, amplifiers and oscillators may form a part of the support electronics so that the transduced signal from the sensor can be readily converted into a suitable form, useful for display or control purposes. Integration of these circuit elements along with the sensor on a single chip (on-chip electronics) has many advantages. Significantly, fabrication of miniaturized smart sensors become possible with improved signal to noise ratio: due to the proximity of the circuit to the sensor element. Despite the advantages, most of the commercially available sensors do not include the on-chip electronics. Instead, the support electronics is provided external to the sensor. Needless to say this practice is inconsistent with the very purpose of using silicon-based microelectronic processing technology for sensor fabrication. Investigations, however, reveal a valid reason for this undesirable situation, explained below.

1.3 Sensors and IC technologies

Although the present day sensor technology is well advanced, regularized approaches do not exist for fabrication processes. Hence, the fabrication processes need to be customized depending on the type of sensor or actuator required. Therefore, the sensor technology relies upon research for its advancement. The progress of research in turn depends upon the availability of resources and customized full fabrication facilities to meet the requirement of fabrication. As a result, sensor research in general, and micromechanical sensor research in particular, is limited to a few groups, who are fully equipped with all the necessary facilities and resources to meet the fabrication requirements. A contrasting but a promising trend prevails in IC fabrication technology. This technology is highly regularized in the sense that varying customer (researcher) needs are met with a single process. This regularized approach has lead to standardization of the process which accounts for its

sophistication in terms of easy accessibility and commercial availability through fabrication services [5, 6]. Such a level of standardization and sophistication is absolutely essential for sensor technology, with its growing importance and potential applications in many areas. Also, it is essential to establish a means for the industries and researchers to utilize a fixed fabrication service to produce various types of sensors and actuators and contribute to the advancement. The most simple and economical solution lies in working out the possibilities of using the IC fabrication technology for the fabrication of sensors and actuators. In this approach it is however, essential to meet the criterion of not altering the IC fabrication processes in any way.

1.4 Research outline and thesis organization

Realizing the need for a regularized fabrication approach in sensor technology, an attempt has been made to develop a single technique for the fabrication of various sensors and actuators. A simple but powerful approach has emerged as a result of this attempt. It is based on two observations. First, it is found that the base for regularization is inherently present in any of the commercial CMOS technology in use today (such as Northern Telecom, MOSIS and Faselec [7]). Secondly, the base could be established simply by introducing additional layout design procedures apart from the standard circuit layout design procedures applicable to the CMOS process. The approach in its practical form encompasses three stages: The first stage consists of forming a suitable layout for the required sensors and the associated circuits using layout design rules. Compatibility with the commercial CMOS process is achieved at this very stage with a *special sensor layout*, designed using the *standard layout layers* supplied by the foundry. To obtain a sensor structure using a CMOS process however, it is found necessary for the *special sensor layout* not to comply with some of the rules for the circuit layout (design rules supplied by the foundry). Layout designs not complying with the supplied design rules do not affect the IC fabrication process and hence, the *special sensor layout* designs do not alter the CMOS

fabrication process sequence. In this sense, the circuit-forming capability of the CMOS process remains intact and hence, for the circuit part of the layout the usual design rules are applicable. Using the proposed approach, the realization of the so called *smart sensors* lies at this very stage of forming a suitable layout design. The approach also contains the idea of regularization and standardization for the fabrication of various sensors and actuators through CMOS technology. The prepared layout designs will be submitted to the CMOS foundry for implementation in the second stage. The level of sophistication in the proposed approach comes through the fact that the designers do not have to be aware of the various process intricacies employed at the CMOS foundry. The outcome of this stage is a CMOS chip with all the necessary basic structure for the sensor and the circuit as defined by the special sensor and standard circuit layout designs respectively. At the third and final stage of the approach, a *post-processing* step is performed, if necessary, to convert the basic sensor structure into a functional sensor structure. The idea behind the post-processing step is to selectively process the basic sensor structure formed on the CMOS chip. The selectivity of the post-processing ensures the preservation of the circuitry formed earlier during the CMOS fabrication process. The simplicity of the post-processing step lies in the fact that it does not require any expensive laboratory facility. As a matter of fact, the approach itself does not require anything more than a layout design station (a graphics terminal with layout design software), access to a commercial CMOS fabrication outlet and a simple laboratory facility, that is available in any North American university. A flow-chart illustrating the approach is shown in Figure 1.1

This thesis describes the outlined approach along with the results on sensors and actuators that have been successfully fabricated and tested. It begins with a brief outline on the history of the CMOS technology followed by the concepts behind the standard and sensor layout designs, formation of various structures using the CMOS process in chapter 2. The fabrication approach with a test example of an integrated humidity sensor with

on-chip circuitry is explained in chapter 3. Chapter 4 introduces the silicon micromachining concepts with the fabrication examples of polysilicon microbridges given in chapter 5. Fabrication of a variety of sandwiched oxide micromechanical structures and functional devices based on thermal effects is described in chapter 6. An analytical model developed to analyse a thermal-based device is discussed in chapter 7, while conclusions are drawn in chapter 8.

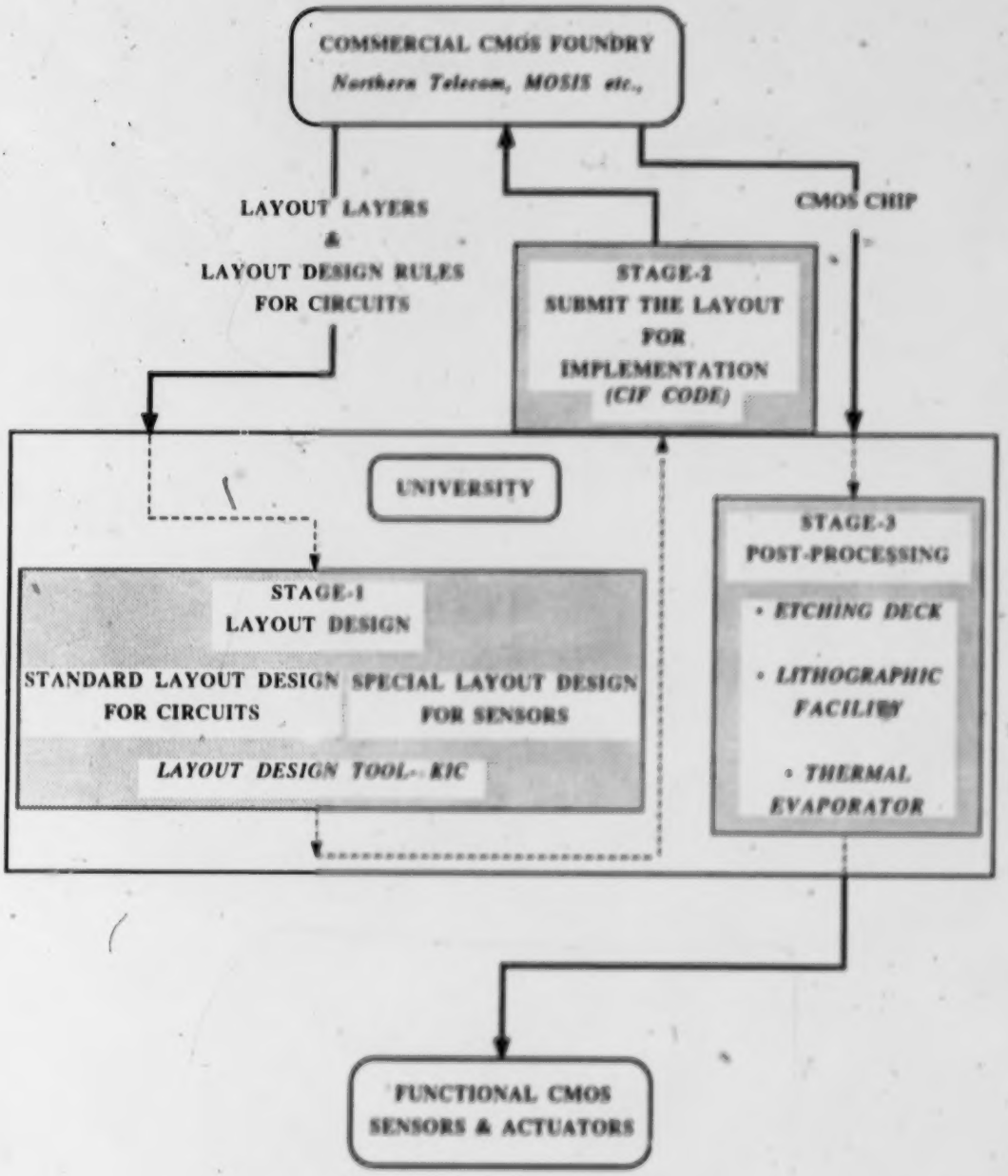


Figure 1.1. Flow chart of the regularized approach.

2. CMOS TECHNOLOGY - AS A BASE FOR MICROELECTRONIC SENSORS

The concept of CMOS technology was proposed in 1962 [2]. However it didn't become very popular until later, during the early '70s. This was mainly due to the assumption that fabrication of two types (p and n-type) of transistors on the same wafer was thought to be technologically incompatible [2]. Furthermore, the attention given to NMOS and PMOS hampered the development of CMOS technology. Later, however, as the power-delay product became an important issue, the advantages of CMOS began to emerge. Since then, the CMOS technology has had to overcome numerous problems towards becoming a leading IC technology [8]. Evolution of CMOS technology involved the adjustment of threshold voltage [8, 9], the layout density increase using the retrograde impurity profile or the twin-tub approach [10], latch-up improvement [11], scaling down of MOSFET device dimensions [12] and hot-electron effects in n-channel devices [13].

2.1 CMOS Process sequence

The most recent CMOS process, popularly known as the twin-tub process, is fabricated using n-tub and p-tub ion implantations into a v-type epitaxial layer. This is followed by twin-tub drive-in, field oxidation, gate oxidation, polysilicon deposition, nonselective P+ source/drain implant, selective N+ source/drain implant, metallization and passivation. The order and the nature of creating various layers (hereafter referred to as *process-layers*) required for the CMOS device is known as the *CMOS process sequence*. The process recipes or the process rules are the result of the research and development that finally established the fabrication technology [1, 2, 8]. Hence, the process rules of various IC industries are usually kept secret, seldom altered and any user-requested process modification is strongly discouraged. Despite this fixed process, CMOS technology is capable of producing various circuits, ranging from simple gates to complex microprocessors. This is achieved by the regularized approach of the CMOS technology.

where the circuit designers are required to submit their ideas in a form which has been so formulated, that the CMOS process sequence is allowed to be kept fixed no matter what type of circuit is being implemented. The method in which the circuit designers supply their ideas to the CMOS foundry is called the layout design.

2.2 Standard layout design rules and circuit formation

Layout design is merely the information that specifies the lateral shapes and the locations of the various process-layers that have to appear on silicon during the IC fabrication process. For each process-layer processed in the CMOS fabrication sequence, there will be a corresponding *layout-layer* available for the circuit designer to specify the lateral shapes and locations of that process-layer [5, 6]. Except for specifying the lateral shapes and locations, the layout supplied by the designer (hereafter referred to as *layout information*) will not influence the nature of the fabrication procedure that creates the corresponding process-layer. In technological terms, the layout information will be used only to pattern the corresponding process-layer lithographically.

Along with the layout-layers, the CMOS foundry supplies a set of rules called *layout design rules* to design proper functional circuits using the layout-layers. Figure 2.1 shows a standard layout design to form an inverter, whose schematic is shown in Figure 2.2. This inverter consists of two transistors, a P-type and a N-type, interconnected electrically. In designing the layout for this inverter, the layout design rules supplied by the foundry have to be strictly observed. Proper definition of the active-area inside a p-well, p+ and n+ layout-layers will ensure the formation of the N-type transistor (see Figure 2.1). Similarly, proper placement of active-area, p+ and n+ layout-layers will ensure the formation of the P-type transistor. Specifying the contact-cuts at the appropriate places and defining the proper metal layer will ensure the proper electrical connection between the metallization process-layer and the transistors formed on silicon. The connection of the functional electrical device formed on silicon to the external world is obtained by bonding a

thin aluminum wire to the metallization layer at an appropriate place. The series of figures shown in Figure 2.3 illustrates the step by step process of the IC fabrication sequence on how the layout information is used to pattern various process-layers and finally obtain the inverter on silicon. The cross-section of the layered-structure formed out of the various process-layers is also shown in Figure 2.3. This type of layered structure forms the fundamental building blocks for sensors in todays sensor fabrication technology. Hence, it should be possible to create various types of layered structures for realising sensors simply by using the layout information in a commercial CMOS technology. These layered structures will be formed out of the process-layers available in the CMOS process, viz., the field oxide, polysilicon, ion-implantations, CVD oxides and metallization and their combination. A set of layout design procedures, called the *sensor layout design*, is developed to obtain several types of layered-structures that are essential for forming a sensor using the commercial CMOS process. These sensor layout design rules are described below.

2.3 Sensor layout design

A sensor layout is the proper definition of a set of CMOS foundry-supplied layout-layers in a particular fashion. The fashion in which the layout-layers have to be defined will be determined from the final layered-structure required to realise a particular sensor. The following sections describe four types of sensor layout design that are employed to fabricate the various sensors and actuators using a commercial CMOS process.

2.3.1 Sensor layout rule 1

Figure 2.4(a) shows a layout design to form a lateral capacitor. The poly-1 is used to form a ground plane and the poly-2 layers are used to form two electrodes. The space between the poly-2 electrodes is exposed to the ambient by the layout-layers contact-cut and

pad-opening defined one above the other. The layered structure formed on a CMOS chip using this layout information is shown in the cross-sectional Figure 2.4(b). In this structure, the capacitance measured between the two poly-2 electrodes was used as a measure to determine the ambient humidity level. The exact details of this humidity sensor are described in chapter 3.

2.3.2 Sensor layout rule 2

Figure 2.5 shows a layout and the corresponding cross-sectional view of a design which will produce a bridge shape using the polysilicon layer available in the CMOS process. The two active-areas defined at locations marked X1 and X2 in Figure 2.5(a) serve as the supports for the polysilicon, while the region between produces the desired bridge shape (see Figure 2.5(b)). With this layout design technique in conjunction with an isotropic oxide etching as the post-processing step, doubly supported, free-standing polysilicon microbridges were fabricated. This is described in chapter 5.

2.3.3 Sensor layout rule 3

Figure 2.6(a) illustrates the third sensor layout, which results in exposing a portion of the silicon substrate to the ambient. This is achieved by defining an active-area, contact-cut and pad-opening one above the other. The layered structure obtained by implementing this layout design is illustrated in the cross-sectional view of Figure 2.6(b). The n-guard and n+ layout-layers shown in Figure 2.6(a) are used to prevent any n-type doping to the active-area during the CMOS process sequence [1, 5].

2.3.4 Sensor layout rule 4

Finally, a portion of the silicon substrate with a surrounding p+ process-layer can be exposed to ambient with the layout design shown in Figure 2.7(a). The desired structure is shown in Figure 2.7(b). The p+ layout-layer is defined to produce a region of p-doped

silicon, which could be used as an etch stop layer during an anisotropic silicon etching step [14]. Typically, in the CMOS process, the source/drain ion-implantations create doping concentrations greater than $5X10^{19}$ cm^{-3} [15], and the literature reports that this level of doping in silicon is sufficient to create an etch stop layer for the silicon anisotropic etching [14].

Using sensor layout rules 3 and 4, along with an anisotropic etching post-processing step, several sandwiched oxide micromechancal structures were fabricated and tested. This is described in chapter 6.

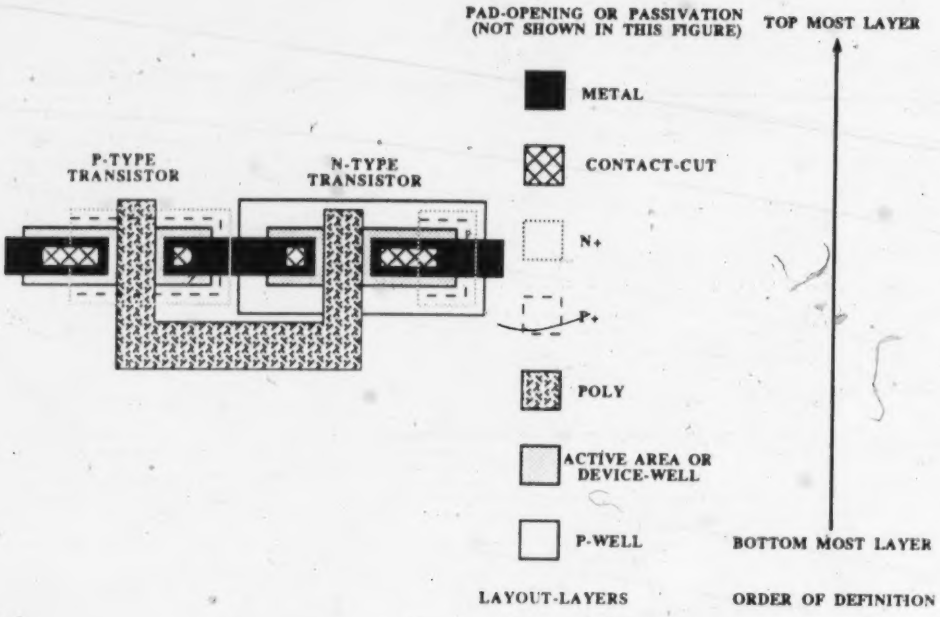


Figure 2.1. Standard layout design for an inverter.

(Legend indicates the name of the layout-layer and the order of definition)

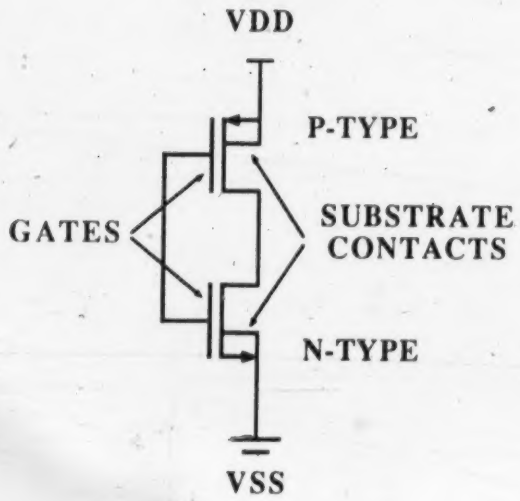


Figure 2.2. Schematic of the inverter circuit.

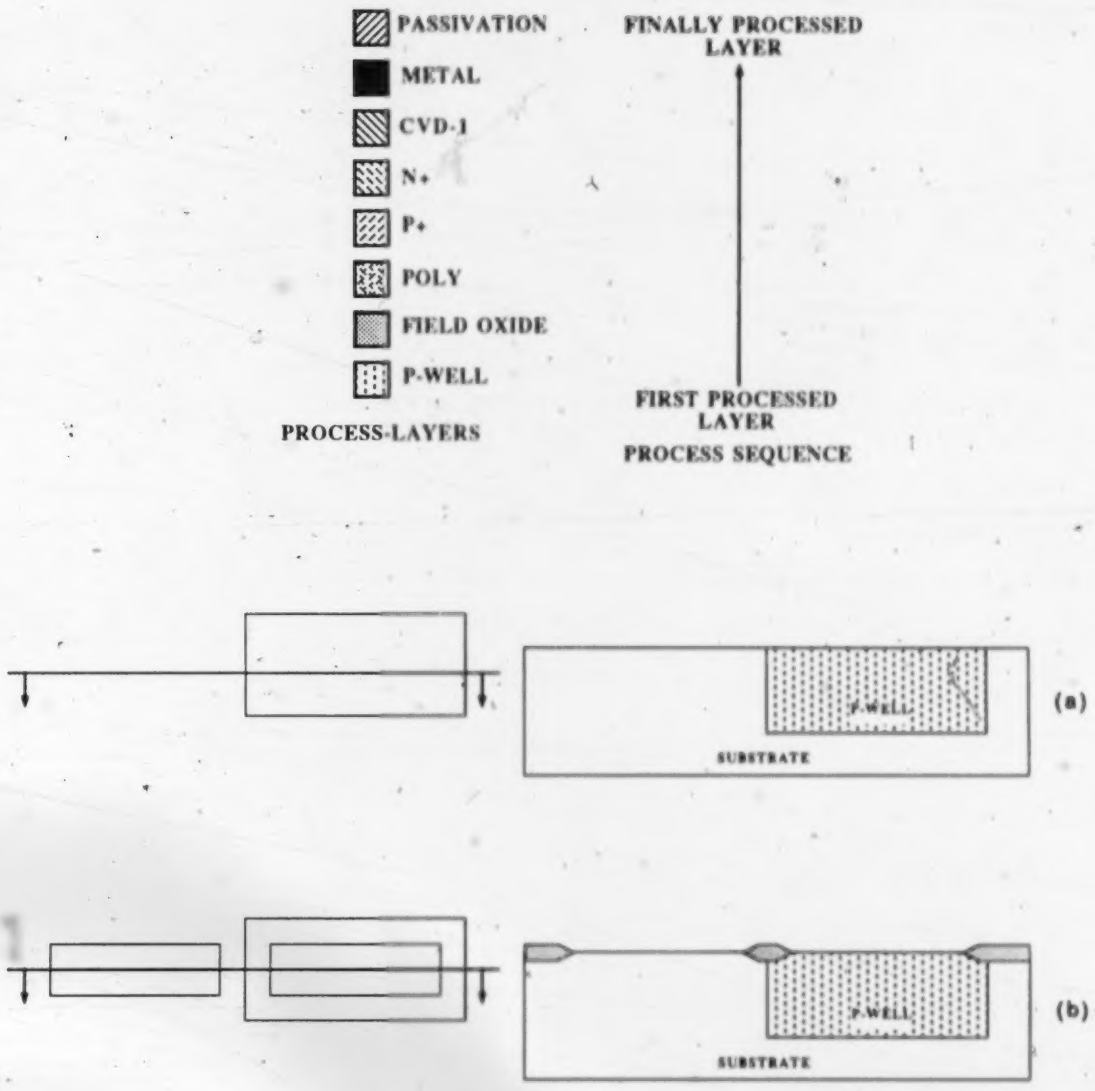


Figure 2.3. Step by step illustration of the formation of the inverter on silicon.

Formation of the process-layers (a) p-well (b) Field oxide

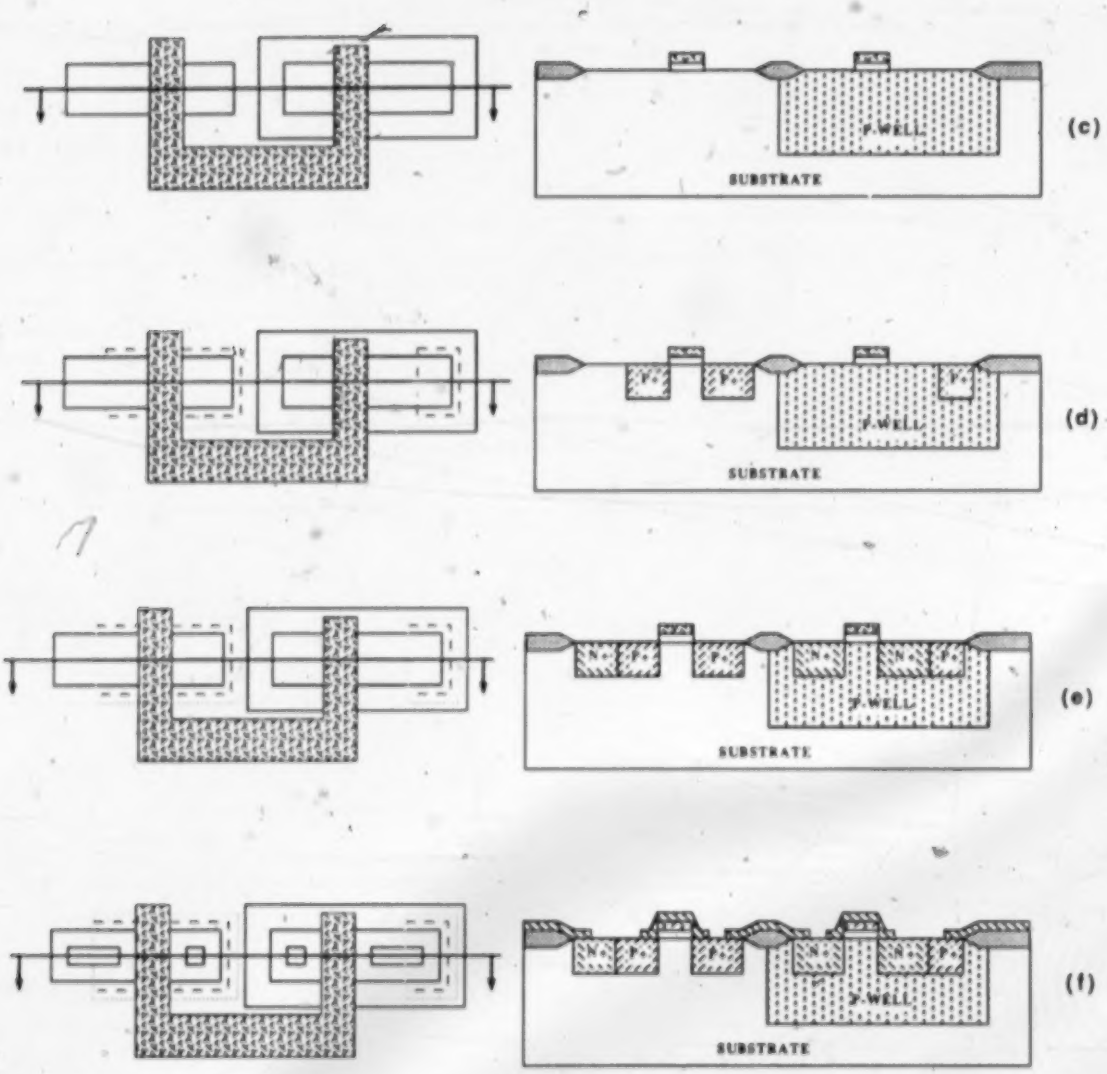


Figure 2.3. Continued. Formation of the process-layers

(c) Polysilicon (d) P+ (e) N+ (f) CVD-1

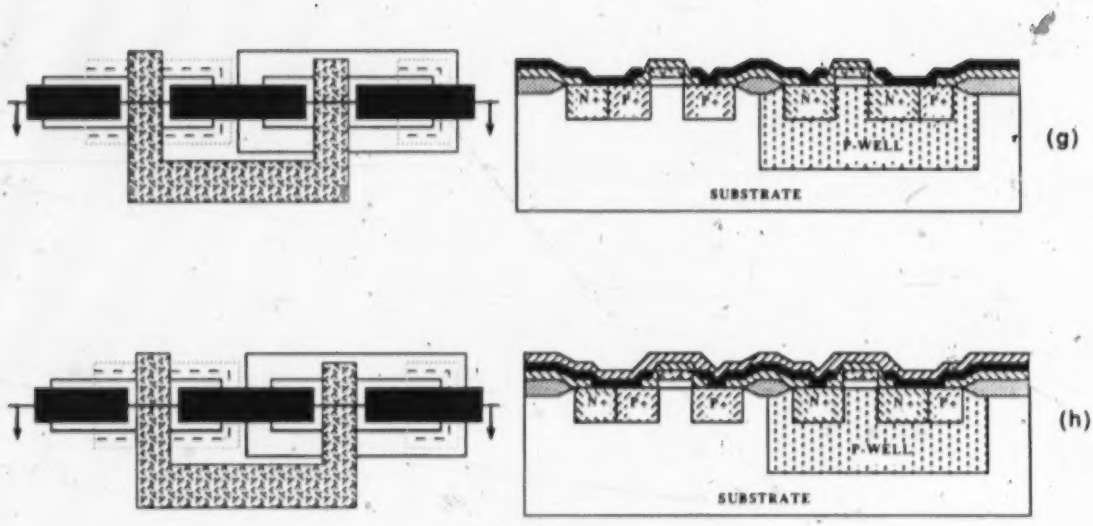
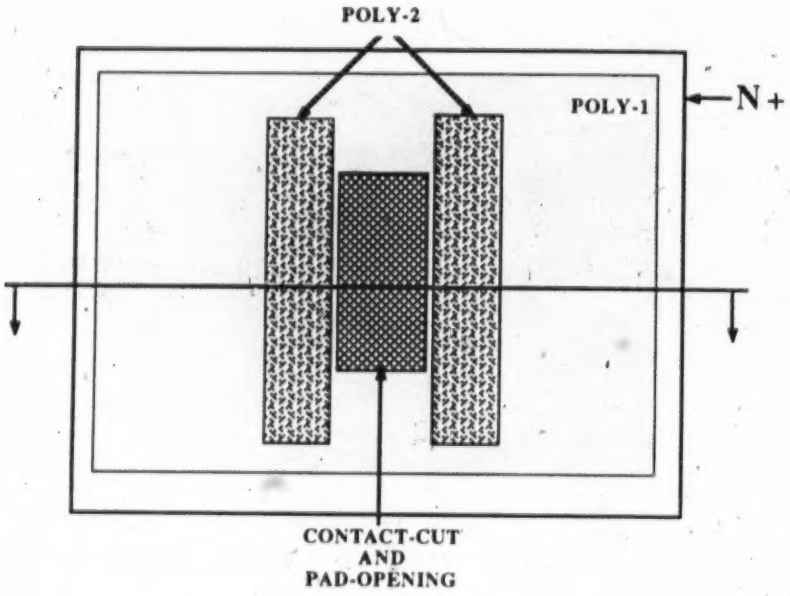
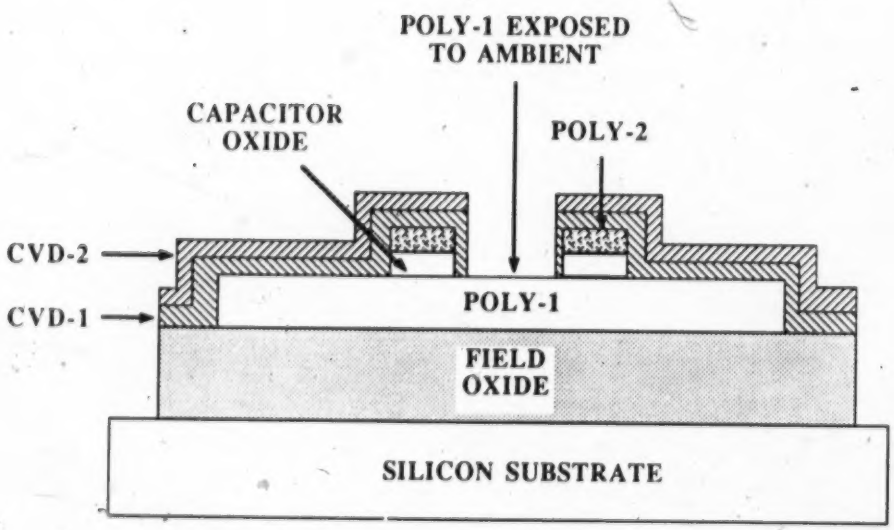


Figure 2.3. Continued.(g) Metal (h) Passivation; the final device structure.

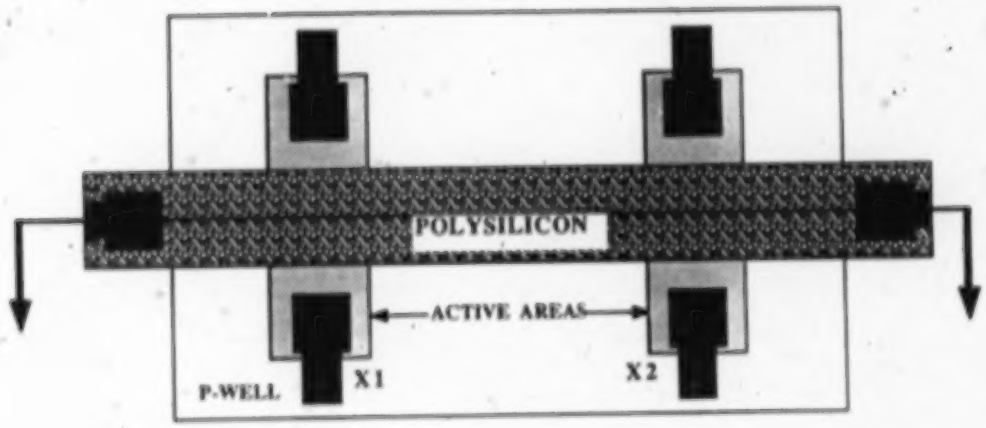


(a)



(b)

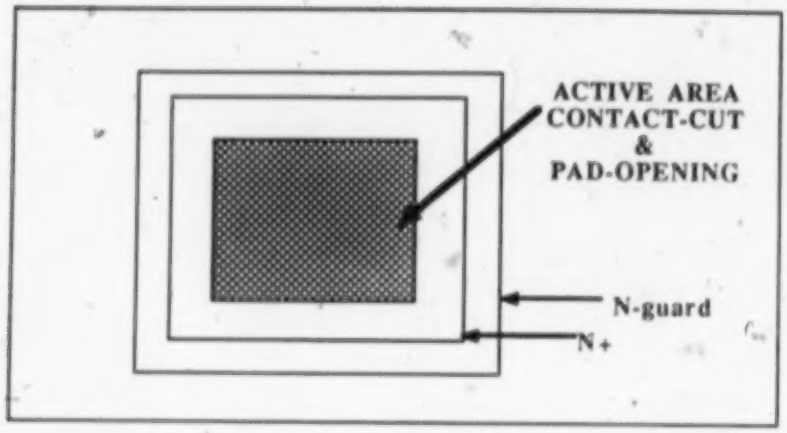
Figure 2.4. Sensor layout rule 1. Design of lateral capacitance structure (a) Layout view (b) Cross-sectional view.



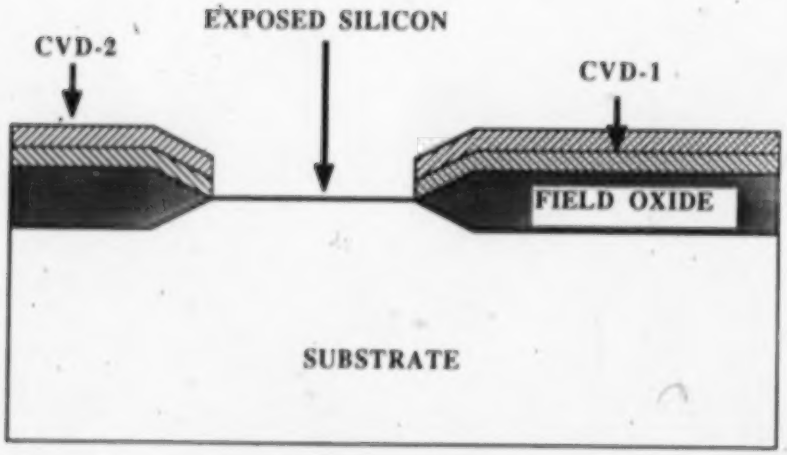
(a)

(b)

Figure 2.5. Sensor layout rule 2. Design of a doubly supported polysilicon microbridge. (a) Layout view (b) Cross-sectional view.

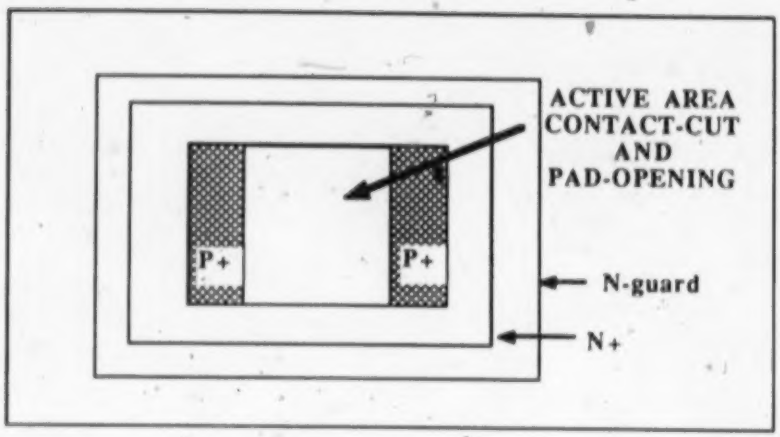


(a)

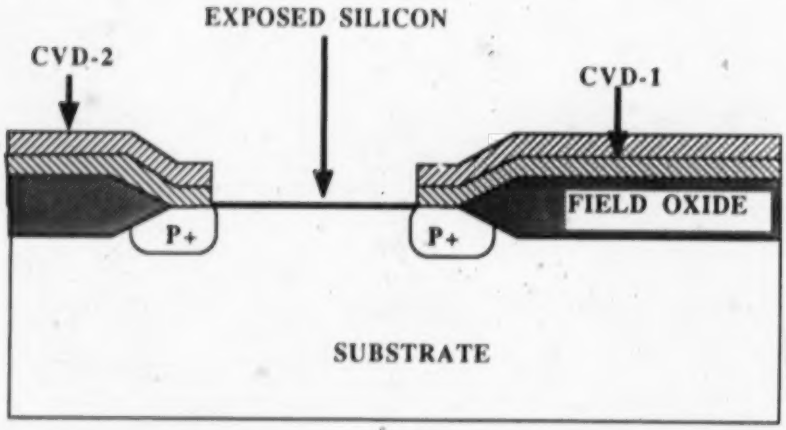


(b)

Figure 2.6. Sensor layout rule 3. Design of a sandwiched oxide micromechanical structure. (a) Layout view (b) Cross-sectional view.



(a)



(b)

Figure 2.7. Sensor layout rule 4. Design of a sandwiched oxide micromechanical structure with P+ etch stop. (a) Layout view (b) Cross-sectional view.

3. CMOS HUMIDITY SENSOR

Humidity control is indispensable in many areas, such as air conditioning, semiconductor fabrication, libraries, textile industries, agriculture and manufacture of chemicals. Along with the growth of integrated circuit (IC) technology, highly desirable miniaturized and integrated sensors are also currently being developed.

3.1 Previous work

Several types of humidity sensors are presently used. Mechanical sensors, though simple and unpowered, suffer from limitations due to their physical configurations and have been found to be unsuitable for many control applications [16]. Optical dew point sensors based on visible or infrared reflection or transmission yield reliable measurement and control. However, their physical size, cost and maintenance have rendered them less attractive for many applications [16].

Attempts to develop microchip humidity sensors using IC technology have produced many types of resistive and capacitive sensors [17, 18, 19, 20]. In particular, polymide-based capacitive sensors and their properties have been studied extensively [20, 21, 22]. Although these sensors solve the problem of physical size, their integration with circuits requires a hybrid IC technology. In order to overcome this limitation, IC process-compatible humidity sensors are being developed. Passive capacitive humidity sensitive elements [23, 24] and active humidity sensitive elements such as floating-gate FET and duplex-gate FET [25, 26] have been reported. However, fabrication of the above-mentioned elements deviates considerably from the standard CMOS processing steps.

Hence, an attempt was made to fabricate a humidity sensor using the standardized approach. The sensor is based on a lateral capacitance structure obtained using the sensor layout rule 1 described in section 2.3.1.

3.2 Design and fabrication

3.2.1 Device structure

Humidity sensors based on capacitance changes are very common. Most of the capacitive sensors are fabricated using the conventional capacitance structure consisting of two parallel electrodes (usually metal) sandwiching a humidity-sensitive dielectric [18]. A conventional capacitance structure can be realised in CMOS technology only if SiO_2 is used as the dielectric, and the CMOS SiO_2 is not porous. We therefore use a different device structure, namely, a lateral capacitance structure, similar to the one reported by Regtien [24]. The electrodes of this capacitor are fabricated in standard CMOS technology and the moisture-adsorbing material serving as the capacitor dielectric is deposited during the post-processing step.

The lateral capacitance structure is designed using the polysilicon layers of Northern Telecom's "CMOS-1B" process [5]. Two such structures are illustrated in Figure 3.1(a), a reference element, R, and a sensor element, S. A 361 x 376 μm^2 poly-1 layer is used as a ground plane, over which a pair of poly-2 electrodes are placed. The poly-2 electrodes are designed to form an interdigitated structure in order to obtain maximum capacitance with minimum die area.

Each poly-2 electrode consists of 9 fingers. Each finger is 10 µm wide and 111 µm long. Adjacent fingers are separated by 9 µm distance. For the sensor element S, eight 5µm x 10µm contact-cuts are made in the space between the fingers to provide a physical opening, as shown in the layout view in Figure 3.1(a). These cuts facilitate the deposition of moisture-adsorbing material in the postprocessing step. They enable the formation of a capacitor with the adjacent fingers of the interdigitated poly-2 electrode pair as capacitor plates and the moisture-adsorbing film as dielectric. A 5µmx111µm pad is opened directly above the contact-cut area in order to remove the passivation layer, which is deposited as a protection layer in any standard CMOS processes. A segment of the sensor element is

shown in cross-section in Figure 3.1(b).

For the reference element R, a similar set of interdigitated poly-2 electrode fingers of the same dimensions, but without contact-cuts and pad-opening, are fabricated adjacent to the sensor electrodes. The reference electrode structure is covered completely with a passivation layer.

3.2.2 Selection of moisture-adsorbing Film

It has been determined that vacuum-deposited dielectric thin films have a columnar porous structure [27]. When these pores are accessible to the atmosphere, they tend to fill with condensed water due to adsorption of water molecules. The amount of water adsorbed is a function of the relative humidity of the ambient air. At lower humidity levels the water molecules condense on the top of the pores. As the humidity level increases, the size of the condensed water droplet increases and a thin sheet of water forms on the top of the porous film. This process is known as monolayer formation [27, 30]. Any further increase in the humidity level, beyond the monolayer formation, forces the condensed water to slowly diffuse into the pores until they are completely filled. This is called the capillary condensation effect [27].

The adsorbed water affects the properties of the columnar film. One such property of interest is the permittivity. Indeed, the change of capacitance with the amount of water adsorbed in deposited films used as a dielectric has been utilised to study the columnar structure of dielectric thin films. For example, investigations of MgF_2 thin films using the so-called "capacity" method have been reported by T. Chudoba [27]. Besides the well documented columnar properties of MgF_2, the ease of its deposition by vacuum evaporation makes it an attractive moisture-adsorbing material for the sensor design.

3.2.3 Post-processing

The post-processing step for the fabrication of the CMOS humidity sensor involves deposition of porous MgF_2 on the die. Chips with 1000 Å and 750 Å layers of MgF_2 as well as chips with no MgF_2 were manufactured to examine the effects of film thickness. The deposition was done using a thermal evaporator. With a base pressure of 10^{-6} Torr, the deposition rate was adjusted to 200 Å/min. The substrate was not heated, in order to increase the porosity of the MgF_2 film [28]. The film is deposited on the passivation layer and in the space between the electrode fingers through the opening (caused by the contact-cut and pad-opening) in the sensor element. The formation of the MgF_2 film over the sensor structure is illustrated in Figure 3.2. The deposited film acts as the dielectric for the capacitor formed by the interdigitated electrode fingers. It is the pores in MgF_2 which create suitable adsorption sites for water molecules. Variation in the amount of water vapour adsorbed alters the dielectric constant of the film and hence the measured capacitance. In order to avoid damage to the bonding wires, an epoxy was used to seal the entire die except the sensing area.

3.2.4 Test circuitry and results

To determine the exact nature of the impedance of the sensors, the samples with and without MgF_2 were connected to a HP 4800A vector impedance meter and the impedances measured between 10 kHz to 500 kHz. The impedance values and the phase angles are listed in Table 1. The phase angle of -90° confirms that the impedance of the sensor element is capacitive in the frequency range. In order to test the sensor element for its performance as a humidity sensor, it was incorporated in an oscillator circuit. We chose the simple and commonly used astable multivibrator in which the frequency of oscillation is a function of resistance and capacitance used in the circuit, expressed by the relation

$$f = 1.46/(R_a + 2R_b)C \qquad (3.1)$$

where R_a and R_b are resistances and C is the capacitance used in the multivibrator design [29]. A discrete hardwired dual multivibrator circuit was built using a dual timer (NE556) chip. Its schematic diagram is shown in Figure 3.3, with indicated values of R_a and R_b in the sensor (R_{as}, R_{bs}) and reference (R_{ar}, R_{br}) section, respectively. In this circuit, we make use of the sensor capacitor element C_s as the variable frequency-determining component in one of the multivibrators and the reference capacitor element C_r in the other. Since the capacitance C_s changes with humidity, the corresponding multivibrator functions as a humidity-sensitive oscillator, while the other acts as a reference oscillator. The variation of the frequencies f_s and f_r, of the two oscillators is given by equation (3.1), with appropriate values of R_a, R_b and C.

The oscillators are placed in an environmental chamber and the capacitor elements exposed to various levels of relative humidity using a Humitemp PCRC-11 HPT electro-humidity controller. The frequency of the oscillators as a function of relative humidity are measured at room temperature using a frequency counter over a range of humidity of approximately 20% to 90%. Figure 3.4 shows the frequency response (f_s) of the humidity-sensitive oscillators as a function of relative humidity for the two MgF_2 film thicknesses, while Figure 3.5 shows the response for the device with no MgF_2 film. The maximum fluctuations of the sensor frequencies that were observed are indicated by the error bars in the two figures. Devices with MgF_2 film exhibited a maximum frequency fluctuation of ± 0.04% while the devices without MgF_2 film exhibited much higher fluctuations; ±1.2% at 28%RH and ±5% at 90%RH. The exact cause of this behaviour is

unclear. Values for the capacitance C_s are calculated using equation (3.1) for each RH level; plots are shown in Figure 3.6 and 3.7. The error bars indicated in Figure 3.7 show the calculated range of capacitance due to the frequency fluctuations.

Since the reference element is covered with a passivation layer and not exposed to the atmosphere, its capacitance should not vary with humidity. The reference oscillator frequency (f_r) was indeed found to be constant, with a value of 22.55±0.01 kHz for all the values of humidity under study. This behaviour is in contrast with the results reported by R. Jachowicz *et. al.*, [20] and is probably due to the thick passivation layer (greater than 1μm) of the standard CMOS process compared to their CVD SiO_2 thickness of 0.2μm. Furthermore, the sensor impedance measurement at higher humidity levels (>90%RH) exhibited a slight increase in the phase angle (≅1°). This is due to the resistive component that is present in the sensor element and is a function of the cleanliness of the sensor surface, similar to the data presented in [24]. The constant capacitance of the reference element with humidity suggests its possible use for compensation of capacitance changes with temperature.

3.2.5 Discussion

Figure 3.4 indicates that the frequency response for devices with 1000 Å of MgF_2 is linear over 70% of the measured range of RH levels, with a sensitivity of 36.5 Hz/%RH. Devices having 750 Å of MgF_2 exhibit linearity over only 60% of the measured range, and a smaller sensitivity of 12.5 Hz/%RH, as observed in the same figure. The devices with no MgF_2 respond with a sensitivity of approximately 170 Hz/%RH over the measured RH range, as shown in Figure 3.5.

The nonlinearity at the lower RH levels in the responses of the devices with a film of MgF_2 may be due to the single layer coverage of the water molecules on the surface of

porous films, known as monolayer formation [27, 30]. This results in smaller changes of capacitance with RH, as shown by the lower end of both response curves of Figure 3.4. Similarly, at higher RH levels, the capillary condensation effect plays a significant role in causing nonlinearity by saturation [27]. However, we observed this effect only in the case of 750 Å devices (see Figure 3.4), presumably because of the availability of fewer pore sites compared to the 1000 Å devices. Since the 1000 Å of MgF_2 will be higher in volume compared to 750 Å of MgF_2, 750 Å devices would have lesser pore sites. Further, the nonlinearities and sensitivity appear to be a function of the film thickness.

It is apparent that deposition of MgF_2 has resulted in two effects. The capacitance observed for the devices with MgF_2 film, compared with those with no film, clearly indicates that the MgF_2 film has become the dielectric for the sensor capacitance, as anticipated. Typical values observed increase from 4 pF to 30-33 pF, as seen in Figure 3.6 and 3.7. The typical eight times increase in capacitance corresponds to the eight times increase in the relative permittivity of the MgF_2 [27]. Secondly, the porous MgF_2 film possibly provides a medium for a controlled adsorption and desorption cycle with much less fluctuation in the response than the devices with no MgF_2 film.

3.2.6 Comparative evaluation of the capacitance ratio

Since the porous MgF_2 serves as the dielectric material of the sensor capacitor, the resulting capacitance will be proportional to the effective relative permittivity of the MgF_2 film. The minimum and maximum capacitance observed due to the ambient humidity will therefore be proportional to the relative permittivity of the porous MgF_2 film when empty of and filled with water molecules, respectively. The effective relative permittivity of the porous MgF_2 dielectric can be obtained using the general formula [27]

$$\varepsilon_{r\,(eff)} = \varepsilon_{r\,(MgF2)}\, q + (1-q)\, \varepsilon_{r\,(water)} \qquad (3.2)$$

where, q is the packing density of MgF_2, with a maximum value of 0.907 [27]. The packing density gives the measure of the porosity in the MgF_2 film [27]. In calculating $\varepsilon_{r(eff)}$ for 0%RH, the pores are assumed to be free of water molecules, while at 100 %RH, they are assumed to be completely filled with water molecules. Substituting for $\varepsilon_{r(MgF2)}$ and $\varepsilon_{r\,(water)}$ values of 8.47 and 80, respectively in equation (3.2), the $\varepsilon_{r\,(eff)}$ at 0 and 100 %RH is calculated to be 7.7 and 15.1 respectively. This results in the ratio of 1.9. Experimentally, the capacitance C_s of the sensor element with 1000 Å of MgF_2 film for 90%RH and 10%RH have been found to be 33 and 30 pF respectively. The ratio of 1.1 between these capacitance values can be compared against the analytical value of 1.9. The ratio calculated using the analytical method shows a slightly higher value compared to the value obtained experimentally. This could be due to the following two reasons; the experimentally obtained value is for the %RH range of 90 - 10 while the analytically calculated range of %RH is 100 - 0 and assumes complete filling of the pores by condensed water. Further, the analytical expression given by equation (3.2) assumes a parallel plate capacitor completely filled with porous MgF_2 as dielectric. However, for the capacitance structure obtained using the CMOS process, there exists a considerable air gap (see Figure 3.2) which would lessen the amount of capacitance change upon water adsorption.

3.3 Integrated CMOS humidity sensor

Since the devices with no MgF_2 film showed response to humidity, the possibility of fabricating an integrated CMOS humidity sensor without the moisture-adsorbing film was attempted. Hence, a multivibrator circuit was proposed and integrated with the sensor element.

3.3.1 Sensor-circuit

The humidity sensor element used in this integrated version was identical to the one described in section 3.1.1, consisting of poly-1 and poly-2 electrodes for lateral capacitance structure. The multivibrator circuit used in our design comprises two parts as shown in the block diagram in Figure 3.8. The first part is a current source/sink with current I_S and the second part is a Schmitt trigger, which uses the humidity sensor element as its timing capacitor with capacitance C_S. The schematic of the circuit with the sensor element is shown in Figure 3.9.

Transistor M1 and the external resistor R establish the constant current I_S. This current is then mirrored by M2-M7 into M8 and M9, establishing M8 as a current source and M9 as a current sink [31]. M10 and M11 function as switches driven in opposite phase by the output of the Schmitt trigger. When M10 is on, the sensor element will be charged with a constant current I_S, producing a rising linear ramp voltage at the input of the Schmitt trigger. When M11 is on (at this time M10 will be off) the sensor element will be discharged with the current I_S producing a falling ramp voltage at the input of the Schmitt trigger. Since the magnitude of the charging/discharging currents are same, viz., I_S, the ramp voltage can be expressed as:

$$|dV_S/dt| = I_S/C_S \qquad (3.3)$$

Transistors M12 through M17 configure the Schmitt trigger [31]. The Schmitt trigger has two output states, 'High' and 'Low'. The 'High' output will be present when the input voltage V_S, goes below the lower threshold (V_{Sl}) of the Schmitt trigger input and the 'Low' output will be produced by the Schmitt trigger when V_S is greater than the upper threshold voltage (V_{Sh}).

At the instant of energizing the circuit, the charge stored on the sensor element is zero and hence the voltage across it is zero. This will cause the Schmitt trigger to assume a 'High' output. This output voltage switches M10 on and the sensor element is charged with I_s, causing the Schmitt trigger input voltage (V_s) to increase linearly until it reaches the upper threshold voltage (V_{sh}) of the Schmitt trigger. When V_s crosses V_{sh} the Schmitt trigger flips its output state to 'Low'. This transition makes M10 switch off and M11 switch on, causing a linear discharge of the sensor element. There is now a linear fall of V_s until it reaches the lower threshold voltage (V_{sl}) of the Schmitt trigger. When V_s crosses V_{sl}, the output of the Schmitt trigger flips the output state to 'High' and the process repeats.

If the width of the Schmitt trigger's hysteresis loop (V_{sh}-V_{sl}), is V_h, then the period for one half cycle of the Schmitt trigger's output for the above circuit is given by

$$T/2 = (V_h C_s)/I_s \qquad (3.4)$$

Hence the output frequency:

$$f_o = I_s/(2 V_h C_s) \qquad (3.5)$$

Since the capacitance C_s of the sensor element is modulated by the ambient RH, the output frequency is a function of the ambient RH, viz.,

$$f_o = f(RH) \qquad (3.6)$$

The entire circuit was simulated using 'SPICE-2' for optimizing the geometric parameters for the circuit elements [32]. The SPICE program listing and the output is listed in Appendix-A. The photomicrograph of the fabricated chip is shown in Figure 3.10.

3.3.2 Experimental testing, results and discussion

The humidity-sensitive multivibrator was exposed to various levels of RH using a Weiss-Technik 305SB environmental chamber. In order to avoid damage of bonding wires an epoxy was used to seal the entire die except the sensing area. The frequency output of the multivibrator was plotted against the RH levels over the range of 15%-95% and a typical response is shown in Figure 3.11. Unlike the discrete version described in section 3.2.4, the humidity sensor under discussion did not exhibit any noticable fluctuations in the output frequency. This may be attributed to the integration of the sensor element and the oscillator circuit on the same chip, reducing the possibility of stray capacitance effects.

Defining the sensitivity as:

$$S = \Delta f / \Delta RH \qquad (3.7)$$

we obtain a value of S = 25.64 Hz/%RH for the region 40-90% RH. A slower response at the lower end of the RH range could be due to monolayer formation [27]. The effect of temperature on the response is shown in Figure 3.12 and it is approximately 50 Hz/°C at 30% RH and 55 Hz/°C at 80% RH and varies linearly.

An interdigitated capacitive element, similar to the sensor element but without the contact-cuts and pad-opening was also integrated with the intention of using it as a reference element with respect to temperature. This reference element also exhibited change in capacitance with RH identical to the sensor element. This could be due to the process modifications incorporated by the CMOS foundry, particularly to the passivation layer.

This effect can be nullified by incorporating proper temperature compensation in the oscillator circuitry. Comparing the effect of the reference element with the previous results (section 3.2.4) it can be concluded that the reference capacitance depends on the specific CMOS process and the temperature compensation has to be incorporated in the circuit. The hysteresis response of the sensor was measured by measuring the response over a closed loop of RH between 20% and 95% (@50°C). This is shown in Figure 3.13. From this we can observe that the hysteresis response is less than 3% of the full range response shown in Figure 3.11.

The above discussions show only the possibility of fabricating an integrated humidity sensor using the standard CMOS technology as a result of a regularized scheme. To enhance the practical and commercial values of the device, a careful choice of a CMOS process becomes necessary. For example, the CMOS process with two levels of poly and silicon nitride as the passivation layer would be an appropriate choice. Studies on the long-term durability are also equally important in the further development of these types of humidity sensors.

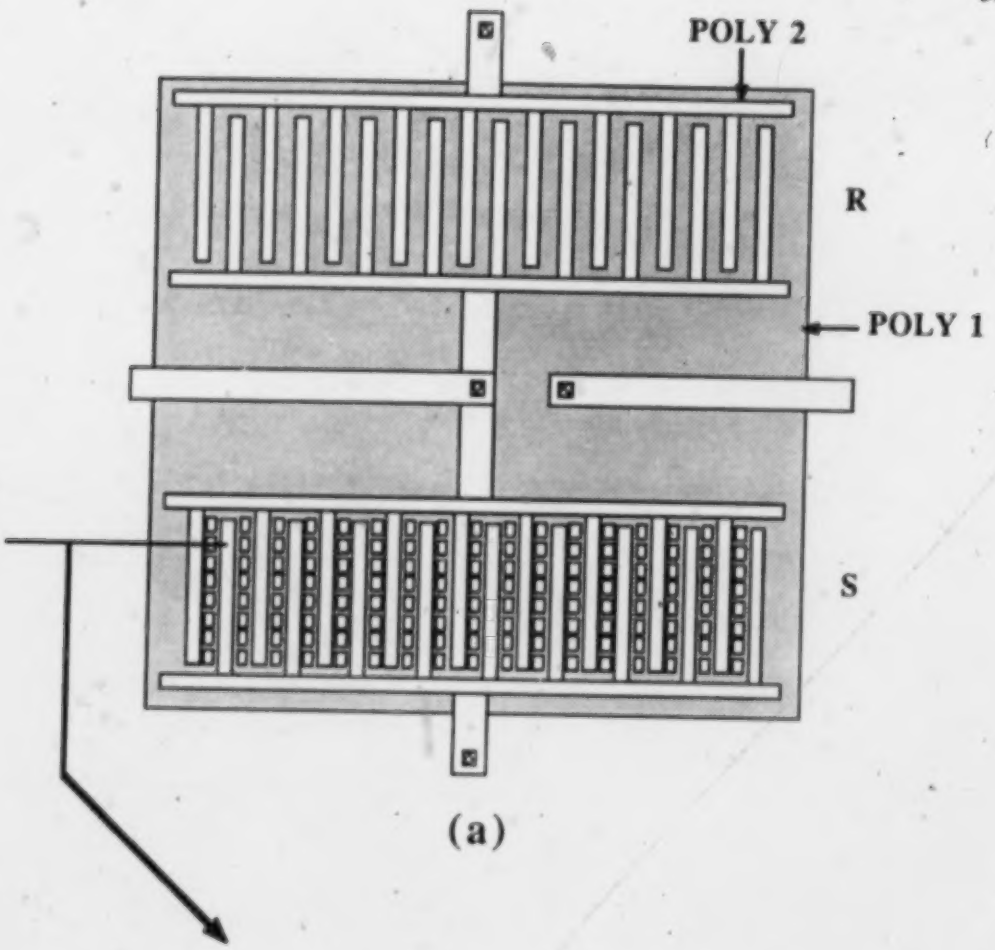


Figure 3.1. Lateral capacitance structure in CMOS 1B technology

(a) Layout view (b) cross-sectional view.

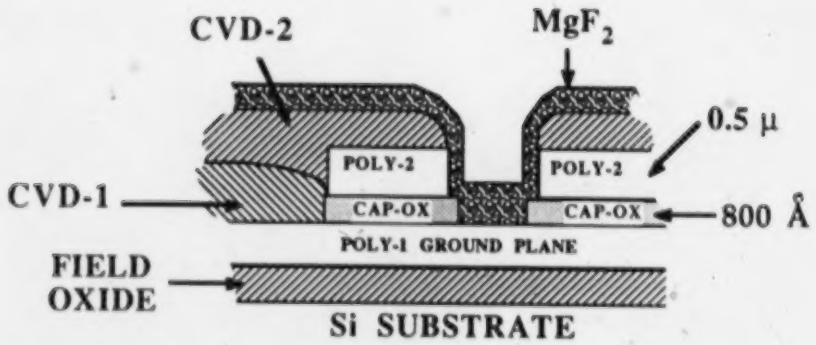


Figure 3.2. Formation of the MgF_2 film over the sensor structure.

Samples with no MgF_2 film

Frequency (kHz)	Impedance (Ω)	Phase
10	3.8×10^6	-90°
50	7.5×10^5	-90°
100	3.7×10^5	-90°
500	8.2×10^4	-90°

Samples with 1000Å MgF_2 film

Frequency (kHz)	Impedance (Ω)	Phase
10	4.1×10^5	-90°
50	8.9×10^4	-90°
100	3.9×10^4	-90°
500	9.1×10^3	-90°

Table 1.

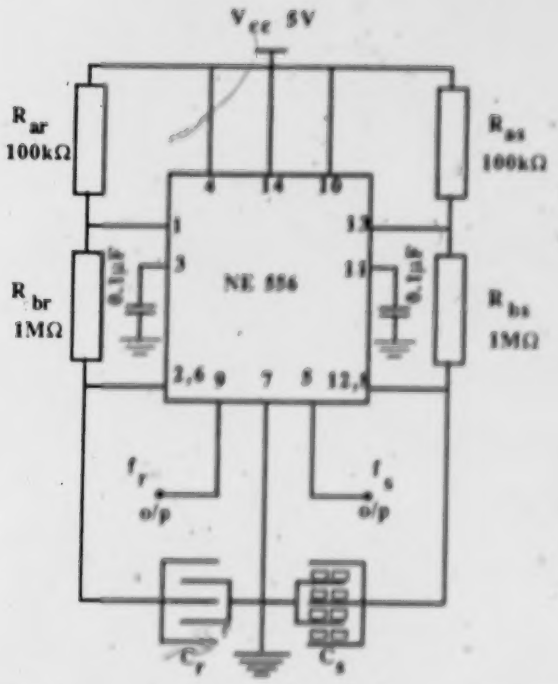


Figure 3.3. Schematic of the oscillator test circuit using 556 timer chip.

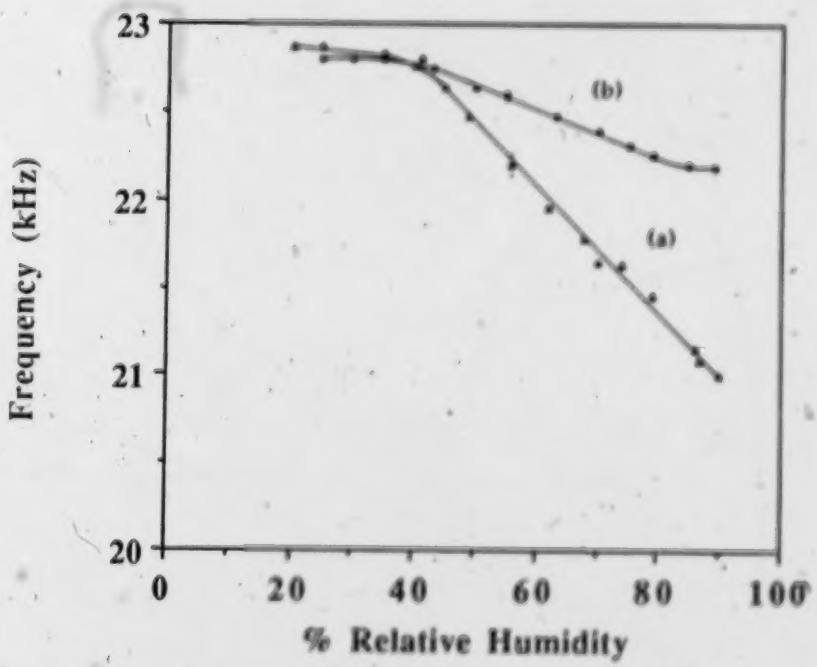


Figure 3.4. Frequency response of the humidity sensitive oscillator with MgF_2 film. (a) 1000 Å (b) 750Å.

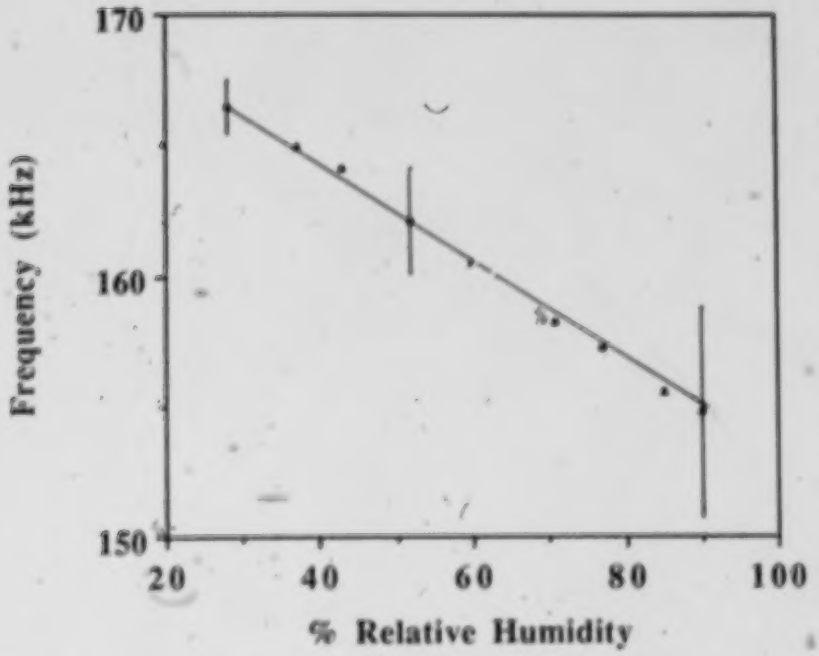


Figure 3.5. Frequency response of the humidity sensitive oscillator without MgF_2 film.

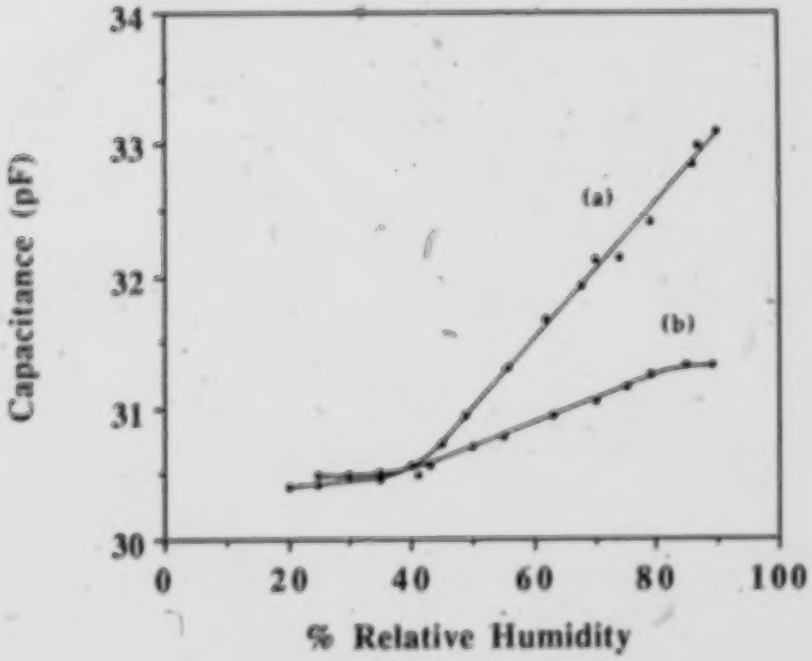


Figure 3.6. Capacitance of the device with MgF_2 film (a) 1000Å (b) 750Å.

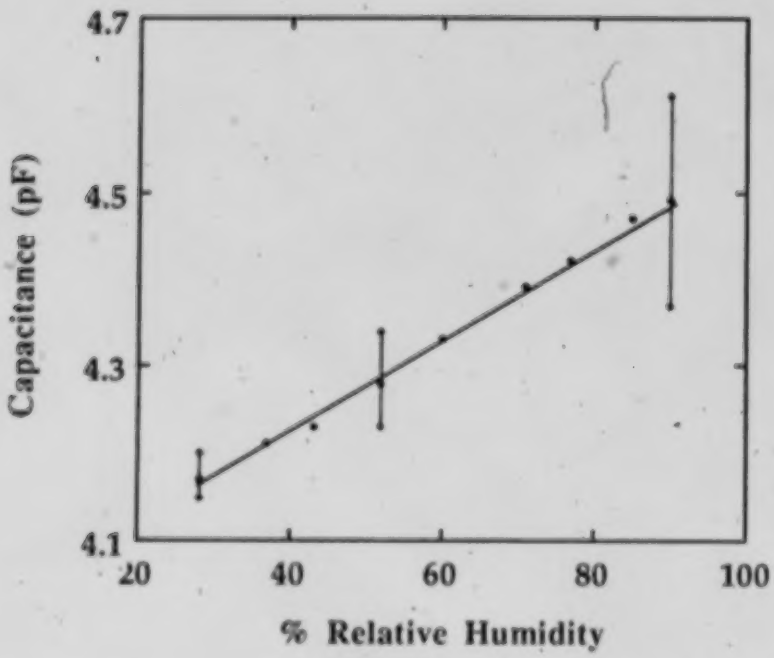


Figure 3.7. Capacitance of the device without MgF_2 film.

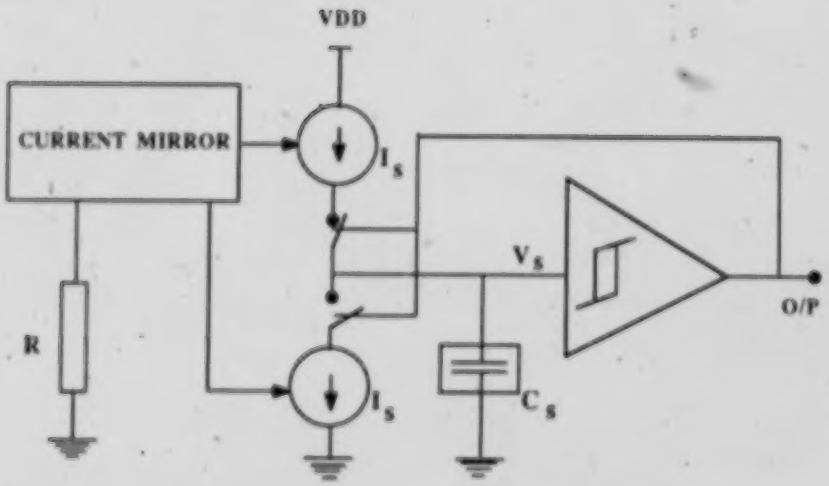


Figure 3.8. Block diagram of the integrated humidity sensitive oscillator.

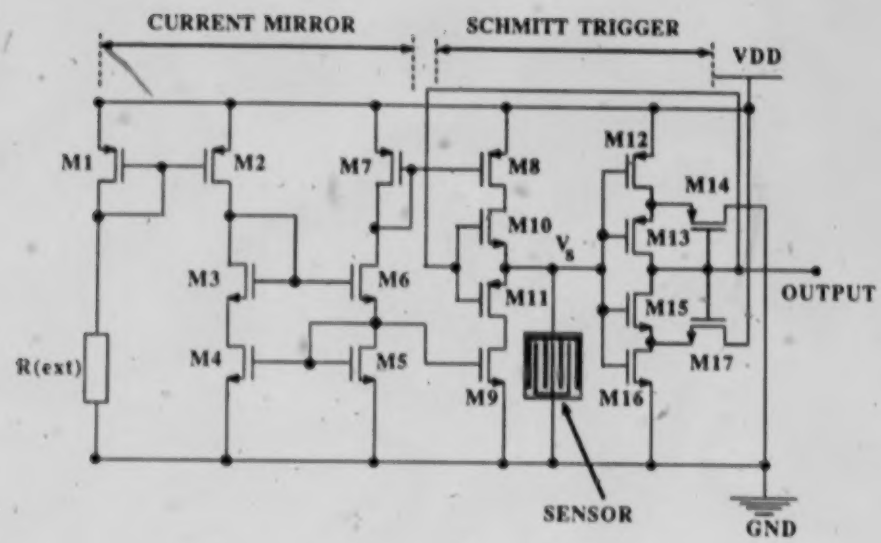


Figure 3.9. Schematic of the integrated humidity sensitive oscillator.

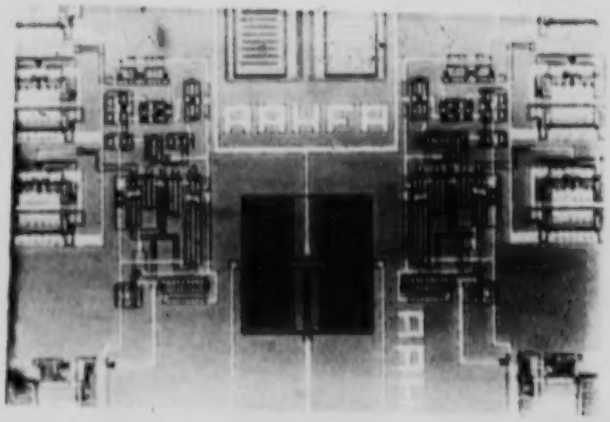


Figure 3.10. Photomicrograph of the fabricated integrated humidity sensitive oscillator.

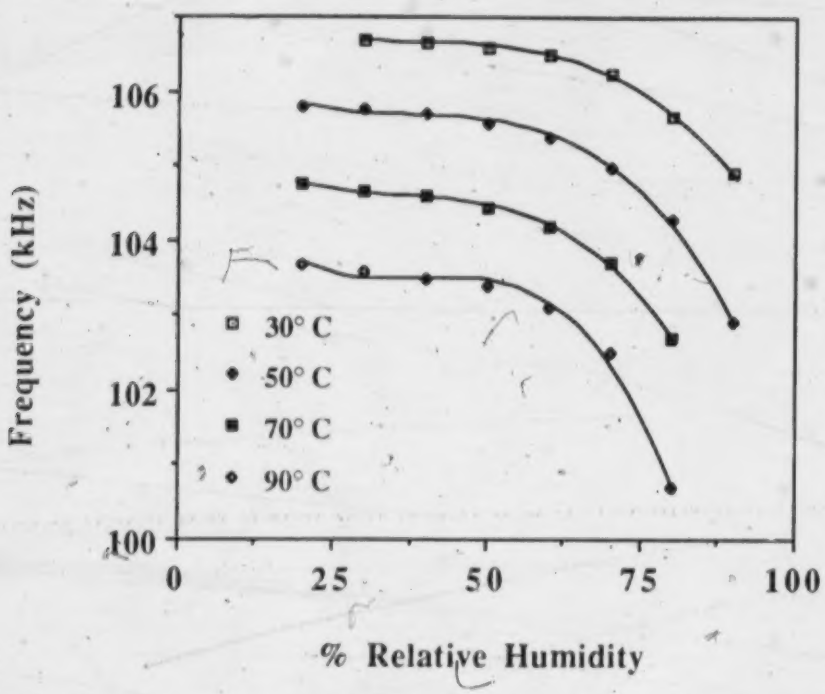


Figure 3.11. Frequency response of the integrated humidity sensitive oscillator.

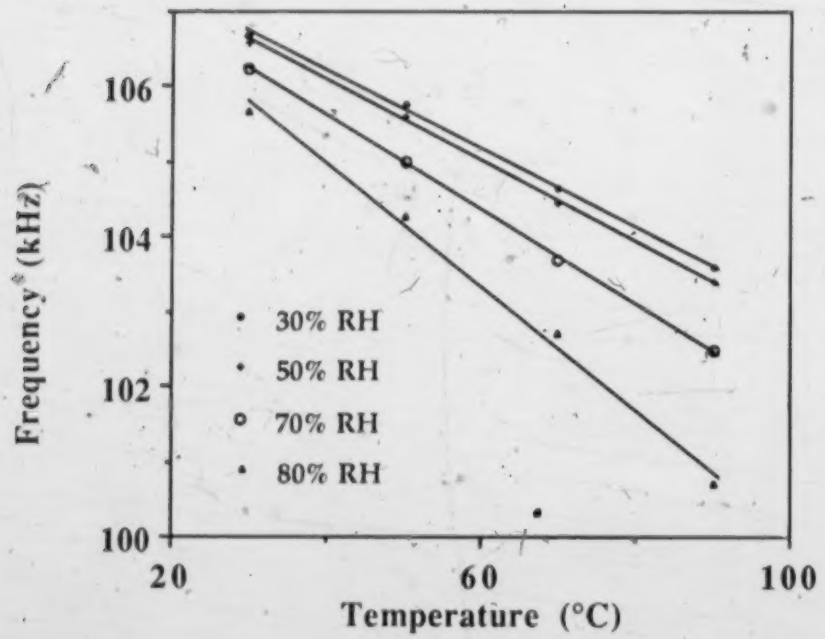


Figure 3.12. Temperature response of the integrated humidity sensitive oscillator.

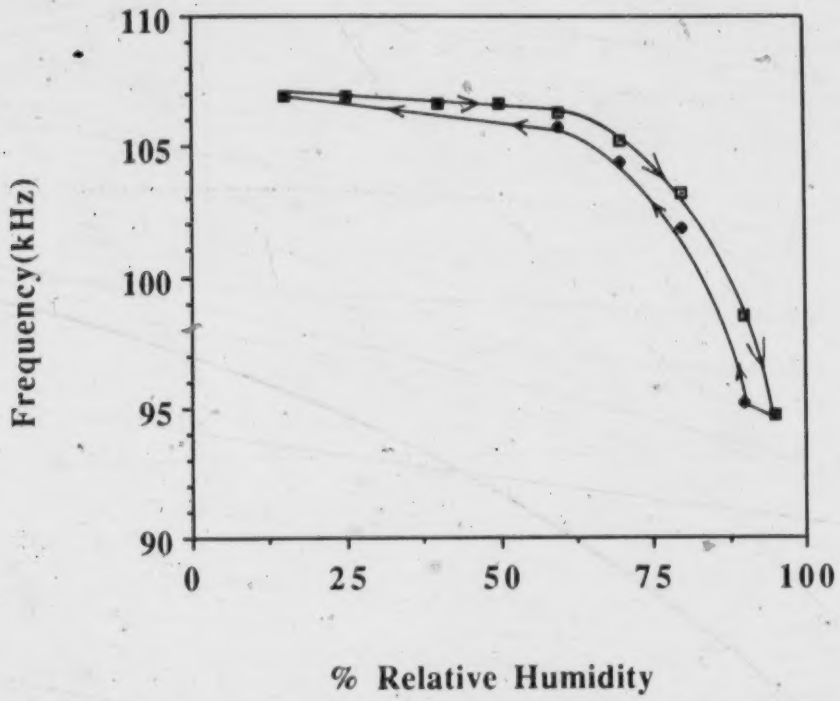


Figure 3.13. Hysteresis response of the integrated humidity sensitive oscillator.

4 SILICON MICROMACHINING

Since the early '70s silicon micromachining technology, the technique of forming well-defined 3-dimensional structures out of silicon, polysilicon and silicon dioxide, have created a major impact in the perception of fabricating microelectronic sensors and actuators [3, 14]. This is due to the fact that favourable mechanical properties of silicon, such as Young's modulus, yield strength and Knoop-hardness, compare favourably to the most popular mechanical material, steel [14]. Although, silicon is brittle and can shatter into pieces if dropped, due to the higher yield strength of silicon compared to steel, a properly mounted silicon mechanical structure can give a much higher mechanical dynamic range for repeated operations. Valves, springs, torsional-mirrors, nozzles, connectors, printer-heads, cantilevers, microbridges, and open and closed diaphragms are some of the micromechanisms that are fabricated using this technology [3, 14, 33, 34, 35, 36]. Silicon micromachining is usually performed by wet chemical etching. There are two types of etching processes very commonly used for silicon micromachining; viz., *isotropic etching* and *anisotropic etching*.

4.1 Isotropic etching

Isotropic etching is the etching process which removes the material equally in all the crystallographic directions of the etched material. This is illustrated in Figure 4.1. As the etchant removes the material and deepens the cavity, it also widens the opening. Isotropic etching has a strong dependence on agitation and this helps the etchant to remove the etched material more quickly and creating a close to hemispherical cavity, as illustrated in Figure 4.2 [14]. Unagitated isotropic etching creates a cavity whose lateral dimensions are greater than the depth (Figure 4.1). This is due to the etchant that is in contact with the bottom of the cavity losing its etching strength as time progresses.

Isotropic etching is usually performed for the fabrication of polysilicon

microbridges, with SiO_2 as the etched material. The popular isotropic oxide etchant is hydrofluoric acid (HF) or buffered hydrofluoric acid, referred to as BOE. Isotropic etching using HF or BOE requires a photoresist mask, to selectively expose only a certain region of the chip to the etchant. The details of the fabrication of polysilicon microbridges using isotropic etching are described in chapter 5.

4.2 Anisotropic etching

Anisotropic etching or crystallographic orientation-dependent etching removes the material at different rates in different directions in the crystal lattice of the material [14, 15, 37]. The three important crystalline planes that play a major role in silicon micromachining are the (100), (110) and the (111) planes [14, 15, 37]. These three planes for a unit cube of a silicon crystal is shown in Figure 4.3 [1]. Anisotropic etching can form well-defined shapes with sharp edges and corners. The most commonly used silicon anisotropic etchants are potassium hydroxide (KOH) and a chemical popularly known as EDP, which is a mixture of ethylenediamine, pyrocatechol and water [14, 15, 37]. For anisotropic etching of silicon, SiO_2 or Si_3N_4 (silicon nitride) is used as the masking material, which will also be part of the final micromechanical structure. Hence, a separate masking step, such as a photoresist mask, is not usually required for performing anisotropic etching.

The type and geometry of the cavity formed by anisotropic etching is determined by the crystal orientation of the silicon wafer surface [3, 14, 37]. The two types of wafers most useful for anisotropic etching are (100) and (110). The (100) and (110) wafers are characterized by the crystalline plane of the surface that is used for processing the circuits. Further, the orientation and shape of the oxide opening on silicon also determines the type and shape of the cavity formed. If a square oxide opening on a (100) silicon wafer is used for the etching, a pyramidal pit will be produced as illustrated in Figure 4.4(a). During anisotropic etching the exposed (100) plane will be etched downward at a constant rate, giving the pit a flat bottom at the start of the etch process. From the edges of the square

opening, four inward-slanting (111) planes (54.7° to the top surface) form the walls of the pit. As the etching continues, eventually the four (111) planes will meet and a sharp point will be formed at the bottom of the pit. At this stage the etching also stops because the anisotropic etching effectively does not attack the (111) planes of silicon. Hence, by varying the dimensions and the shape of the opening, a truncated pyramidal pit with a flat bottom and a trench can be created [3]. These structures are illustrated in Figs. 4.4(b and c).

4.3 Micromachining technology

The basic structural materials that are used for producing silicon micromechanical devices are silicon, silicon dioxide and metallization for interconnects. Deposition or growth of the above mentioned structural material in conjunction with photolithographic patterning are used to form a basic structure [1]. Finally, the unique step which characterizes the silicon micromachining technology, the isotropic or anisotropic etching, will be performed to create a free-standing, three dimensional micromechanical device from the structural material formed during the previous process.

Section 2.3 of this thesis described how different types of layered structures can be created using the CMOS process. Also, the layered structure formed by the CMOS process will consist of silicon, silicon dioxide and metallization. Hence, the basic building block for producing micromechanical structures can be fabricated by implementing the special layout design described in section 2.3. The silicon micromachining step can be performed after the CMOS process as a post-processing step to create the three dimensional micromechanical structure. This approach would allow the fabrication of micromechanical structures using the commercial CMOS process, at the same time retaining the circuit-forming capability of the CMOS process, as described in the section 2.2. Hence, fabrication of micromechanical structures with on-chip circuitry is possible using the commercial CMOS process.

4.4 Selectivity and etch stop mechanism

In any etching process the etch rate and the etch stop are important factors which determine the dimensions and geometry of the etched cavity. In isotropic etching, usually the etch stop will be performed by timing the etching process [38]. This timing is very crucial because any increase in the etch time would enlarge the cavity or remove more material than required and render the device unusable. In anisotropic etching the etch time is not that critical because the shape of the cavity will be bound by the (111) planes and when all four (111) planes meet the etch rate in essence falls to zero [14]. However, if a special shape of cavity is required using anisotropic etching, several etch stops can be introduced. Heavily boron-doped regions serve as etch stops for EDP; selective ion implantation can be used to create this type of etch stop [14]. The other popular etch stop is electrochemical etching, where an electrical potential applied to a certain layer or region of the silicon substrate can be used to create an etch stop for anisotropic etching and form membrane-type micromechancial structures [38]. When using a standard CMOS process for micromechanical structure fabrication, only a heavy boron-doped etch stop can be formed. Boron is the common p-type dopant in the CMOS process [1].

4.5 Alignment

Accurate alignment of the oxide opening on the silicon wafer is essential for the anisotropic etching to create pyramidal cavities bound by the four sides of the oxide opening. This is usually accomplished by placing the straight sides of the opening either parallel or perpendicular to the (110) edge of the silicon crystal, usually parallel or perpendicular to the primary flat of a silicon wafer [2, 5, 6]. Any misalignment causes under-etching until the anisotropic etchant meets the (111) planes. This under-etching can, however, be used for the fabrication of several micromechanical structures. These micromechanical structures are described in chapter 6.

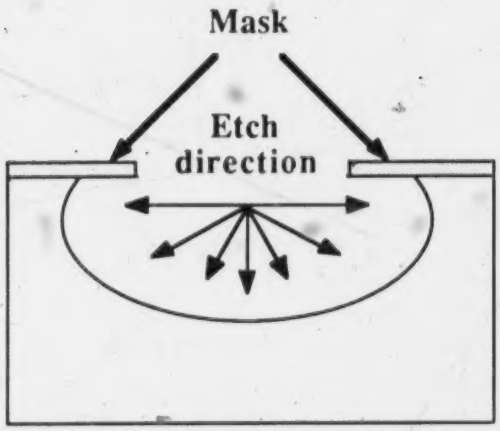


Figure 4.1. Illustration of isotropic etching.

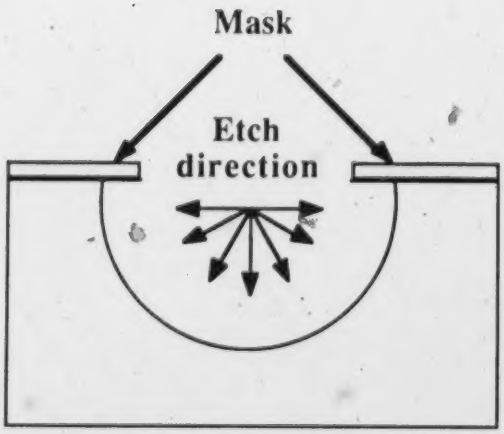


Figure 4.2. Effect of agitation on isotropic etching.

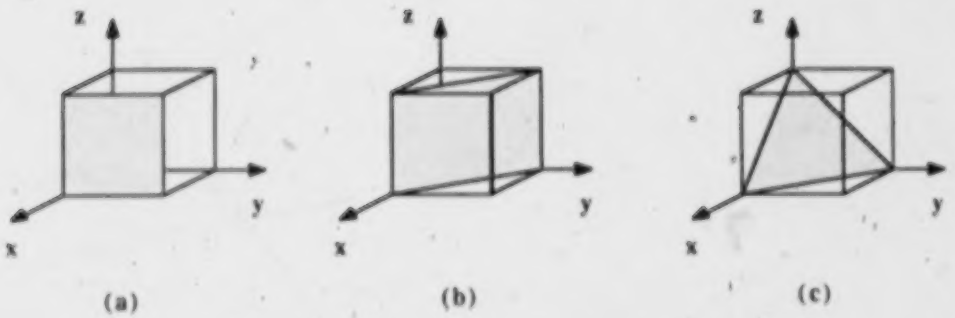


Figure 4.3. (100), (110) and (111) planes of a unit cube silicon crystal.

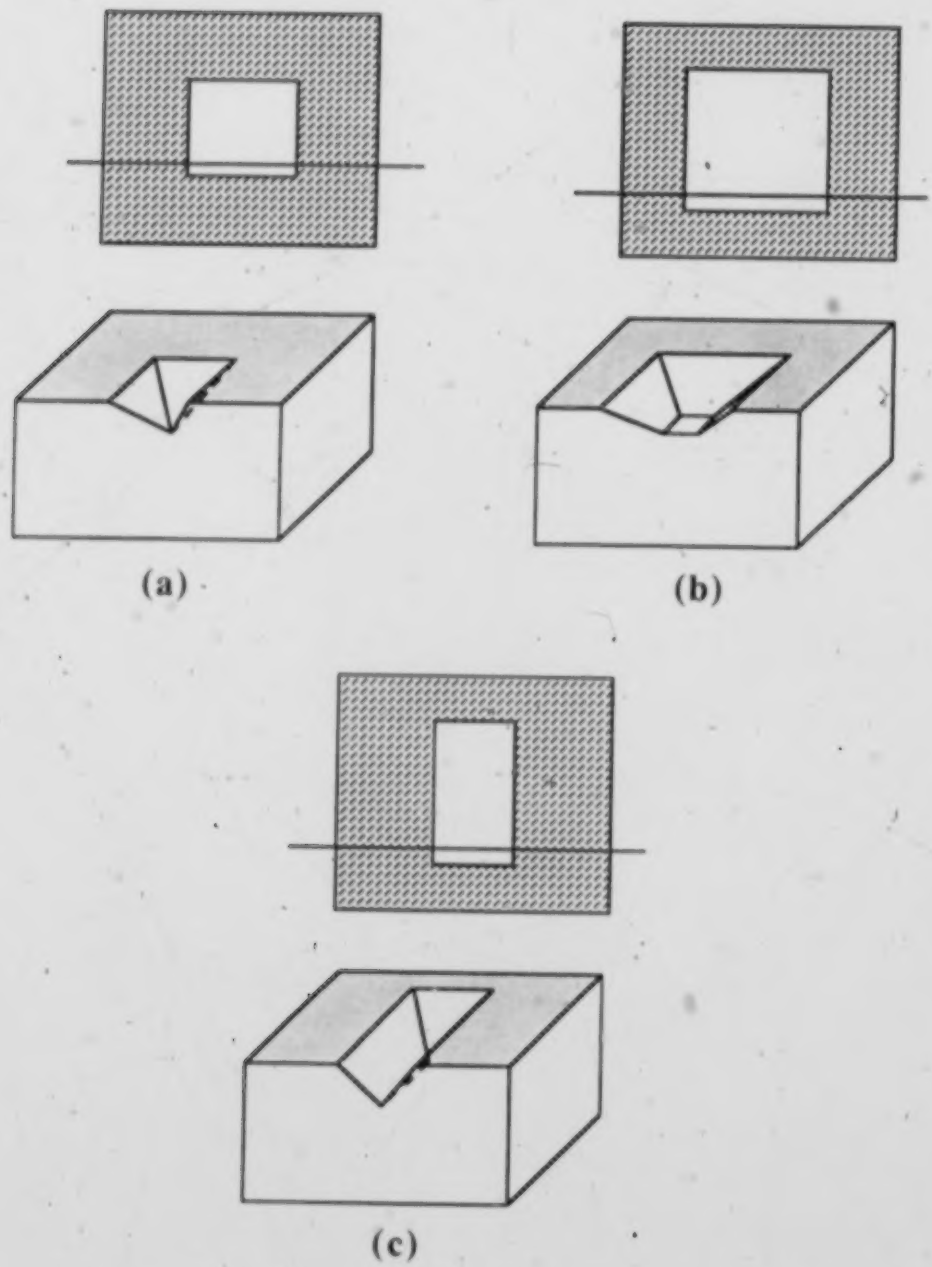


Figure 4.4. Illustration of anisotropic etching. Formation of a (a) pyramidal pit (b) truncated pyramidal pit (c) trench on a (100) silicon wafer.

5. POLYSILICON MICROBRIDGES

One of the most versatile layers in the CMOS process is polysilicon. Polysilicon was introduced as the gate material in the mid '60s for MOS transistors [39]. It allowed the formation of self-aligned transistors, one of the main factors contributing to CMOS achieving high component density. Furthermore, polysilicon permitted the CMOS foundry to easily adjust the threshold voltage of the transistors just by varying the ion implantation dosage [1, 39, 40]. Polysilicon also serves as the resistive element and interconnect material in CMOS circuits.

Besides these advantages, polysilicon also possesses many mechanical properties favourable to the formation of micromechancial structures. The CVD process which deposits polysilicon usually has an excellent step coverage, giving the basic shape for the fabrication of microbridges [39, 41].

5.1 Previous work

The standard approach to date for the fabrication of a polysilicon microbridge [34] is illustrated in Figure 5.1. Initially a layer of oxide (SiO_2 or phosphosilicate glass) is deposited on a silicon substrate and patterned lithographically, as shown in Figure 5.1(a). This is the sacrificial oxide layer and its thickness determines the spacing of the microbridge from the base (substrate). Polysilicon (microbridge material) of the required thickness is then deposited and patterned, see Figure 5.1(b). Next, CVD-1 oxide is used to define the contact area between polysilicon and metal, followed by a metal and CVD-2 oxide deposition, Figs. 5.1(c) and (d). CVD-2 serves as a protection for the metallization layer. Finally, an isotropic etching of the oxide is performed at the polysilicon area where the microbridge is desired. The isotropic etching removes the oxide below the polysilicon and releases a free-standing structure, illustrated in Figure 5.1(e). In this fabrication process, after patterning the polysilicon (step 2 of Figure 5), an annealing step is carried

out to eliminate or reduce the built-in stress developed in the polysilicon during deposition. This annealing step is essential to prevent any deformation of the bridge structure [34, 42].

Examination of the processing sequence described in Figure 5.1 shows that steps 1 to 4 are inherent in any standard CMOS process. The lateral shape of the polysilicon and the desired bridge shape can be specified by sensor layout rule 2; described in section 2.3.2. The final step (step 5), namely the isotropic etching, not available in the standard CMOS sequence, can be performed as a post-processing step to finish the fabrication of the polysilicon microbridge. Since the isotropic etching step requires a photoresist mask, the circuitry fabricated in the CMOS process is protected from the etchant. Hence, the final device includes a polysilicon microbridge together with any desired support circuitry fabricated in the CMOS process. It is important to note that the thickness of the polysilicon is limited by the polysilicon process given in the CMOS sequence, and the spacing between the microbridge and the substrate is given by the thickness of the field oxide.

5.2 Poly microbridge in CMOS technology

Fabrication of poly microbridges using a standard CMOS technology is achieved in three steps: the design of a suitable layout; its realization in a standard CMOS process; and finally the isotropic etching.

A typical sensor layout design for the fabrication of poly microbridges is shown in Figure 5.2(a), where two active regions are defined, and a polysilicon strip placed across them. In the cross-sectional view, Figure 5.2(b), one can see a thin gate oxide beneath the polysilicon in the active areas, with a thick field oxide beneath elsewhere. During the standard CMOS processing sequence, layers of SiO_2 (CVD-1), metallization and passivation (CVD-2) will follow the deposition of polysilicon. The CVD-1 and CVD-2 can be removed during the CMOS process itself by placing a contact-cut and pad opening above the polysilicon at the location where the microbridge is desired. The contact-cut and pad-opening must be over-sized in order to permit the isotropic oxide etchant to remove the

field oxide underneath the polysilicon and thereby form the microbridge, as illustrated in Figure 5.3.

In the CMOS process, the MOSFETs are formed by the self-aligned gate technique. During the source and drain formation steps, the gate material (polysilicon in this case) is also exposed to ion implantation [1, 2]. This is undesirable for the fabrication of microbridges because the ion implantation produces physical damage to the polysilicon [1]. To avoid this, the region of polysilicon intended to form the microbridge is masked from ion implantation with the proper use of p+ and n+ mask layers [5]. Figure 5.4 shows a SEM photograph comparing test microbridges formed out of polysilicon with and without ion implantation. In the lower right of the photograph, a free-standing microbridge is seen, formed from polysilicon that has not been implanted. The ion-implanted polysilicon, in contrast, failed to produce a complete bridge because of the damage caused by the implantation process. Such an unsuccessful bridge is seen in the upper left of Figure 5.4.

Hence, all the requirements for the fabrication of the polysilicon microbridge, except the final isotropic etching, have been achieved by the layout design and no modification to the CMOS process sequence is necessary.

5.3 Post-processing for poly microbridge

The release of the free-standing microbridge is performed by a lithography and etching step after the CMOS processing sequence. This includes spinning the die with photoresist, soft-baking for 45 seconds at 90°C and creating an opening directly above the microbridge (see Figure 5.3(a)). Isotropic etching of the oxide below the poly is performed with a buffered oxide etch (BOE). Depending on the bridge geometry, the etch time required is between 35 and 45 minutes at 27° C. Figure 5.3(b) illustrates the final polysilicon microbridge structure. Figure 5.5 shows a SEM photograph of an unappertured polysilicon microbridge of dimensions 10 μm x 70 μm. Apertures can be introduced to the microbridge by the layout design and the SEM photograph of one such microbridge with

four apertures fabricated using our technique is shown in Figure 5.6. The dimensions of the microbridge are 30 μm x 100 μm and the size of each aperture is 10 μm x 10 μm. Since the lithographic step allows only the selected regions of the CMOS chip to be processed by the isotropic etchant, the circuits or other electrically functional devices formed elsewhere on the chip will be protected from the isotropic etchant. This will ensure the preservation of the circuits formed during the CMOS process, which could be the support electronics for a sensor system realised out of polysilicon microbridges.

5.4 Stress-relief considerations

Built-in stress in CVD thin films is common and requires due consideration [34, 42], otherwise the resulting bridge structure could exhibit buckling or some other deformation. One of the techniques to relieve built-in stress is high-temperature annealing. The exact temperature and duration of the annealing depend on various factors such as deposition temperature, thickness of the film and dopant concentration and must be determined experimentally [43]. The two high temperature diffusion cycles (990° C for 45 minutes and 925° C for 30 minutes) carried out in the CMOS3 DLM process [44], after the deposition of polysilicon, help to relieve the built-in stress in the polysilicon. Such temperatures and durations compare well with the annealing data reported previously [45, 46].

In our experiments, we observed the polysilicon microbridges of length greater than 110 μm failed to produce free-standing structures. Even when proper annealing produces stress-free polysilicon, deformation of microbridges, particularly collapsing of the microbridge, can still occur due to factors such as inappropriate thickness and length of the microbridge or type of isotropic etchant [42, 47]. One common cause of the collapse of microbridges and cantilevers is due to the bending moment caused by the structural parameters [42]. For stress-relieved (through high temperature annealing) polysilicon microbridges the freestanding distances as a function of the thickness of polysilicon have

been calculated experimentally and reported by R. T. Howe [42]. The maximum free-standing length for a 0.5 μm thick annealed polysilicon microbridge is 110 μm. This figure is in close agreement with the 120 μm obtained in our experiments (the thickness of Northern Telecom CMOS polysilicon is 0.5 μm [44]). Figure 5.7 shows a collapsed apertured microbridge of length 120 μm. After collapse, this microbridge does not exhibit any periodic buckling which is the characteristic of an internal stress-free structure [42]. The width of the microbridges does not contribute any significant effect on the free-standing length [42].

5.5 Documented applications

The use of polysilicon micromechanical structures is very attractive in view of the favourable mechanical properties of the polysilicon material. One interesting application of polysilicon microbridges is the vapour sensor, such as those designed by R. T. Howe [35, 42]. This type of vapour sensor makes use of the resilient, deformable mechanical property of polysilicon to detect changes in the mass of the microbridge itself caused by adsorption or desorption occurring in the ambient vapour. The selectivity to a specific vapour is achieved by a dedicated coating applied on top of the polysilicon microbridge. Similar vapour sensors may in the future be fabricated using standard CMOS technology. Other sensors such as anemometers described in [46, 48] could also be fabricated along these lines. Another interesting aspect of CMOS polysilicon is its capability to form resistive elements [5, 39, 40]. The layout designer can form polysilicon layers with four different resistivities just by selecting suitable ion implantation mask layers. A resistive element can be used as a heater, sandwiched between the oxide layers and suspended above a cavity formed by the anisotropic etching to function as an gas-flow sensor [49]. This type of sensor is described in the next chapter.

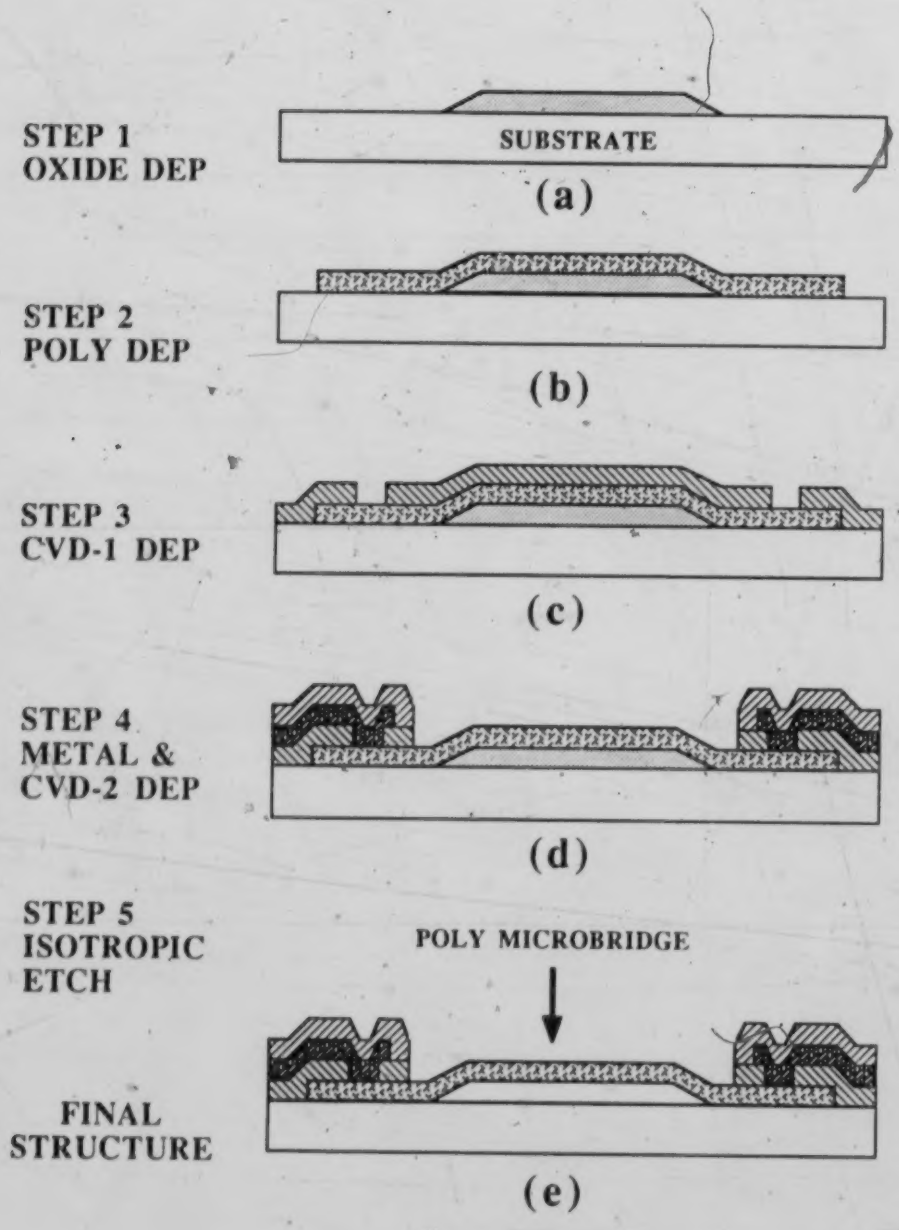
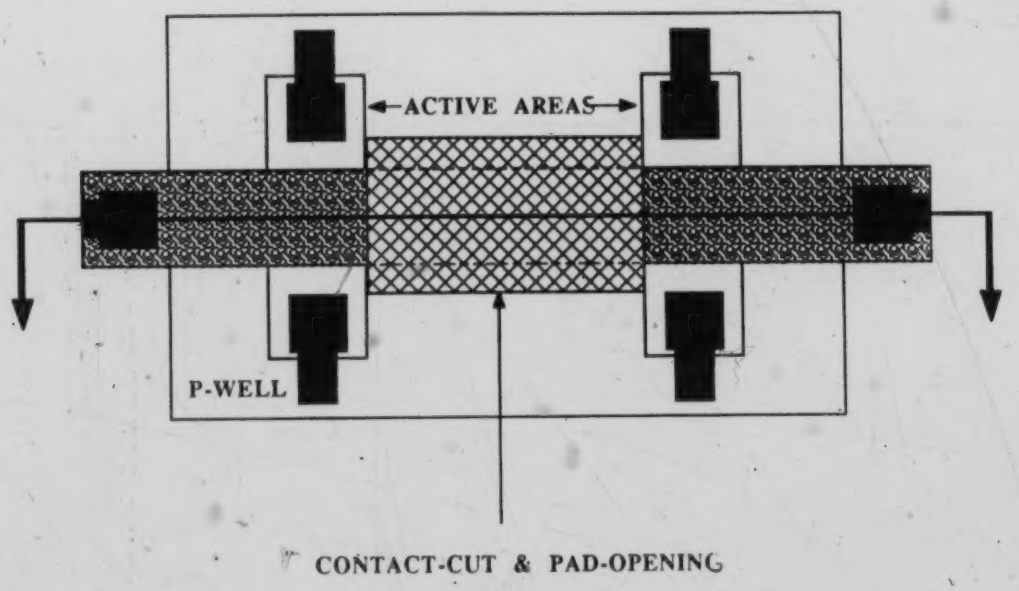


Figure 5.1. Standard polysilicon microbridge fabrication sequence.



(a)

(b)

Figure 5.2. Sensor layout design for the fabrication of polysilicon microbridge in CMOS process. (a) layout view (b) Cross-sectional view.

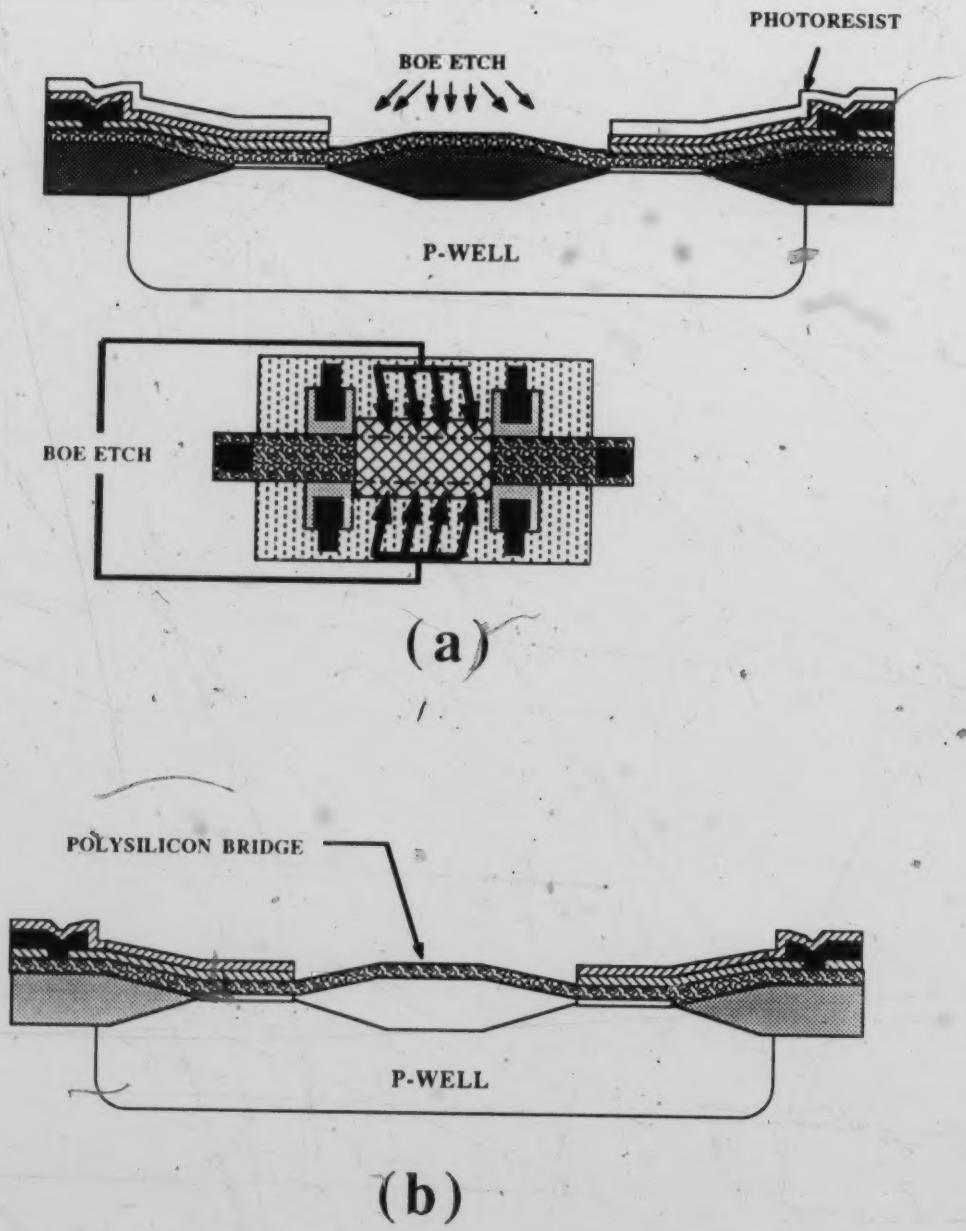


Figure 5.3. Post-processing for the CMOS polysilicon microbridge.

(a) Lithographic and isotropic etching step (b) Completed microbridge; illustration.

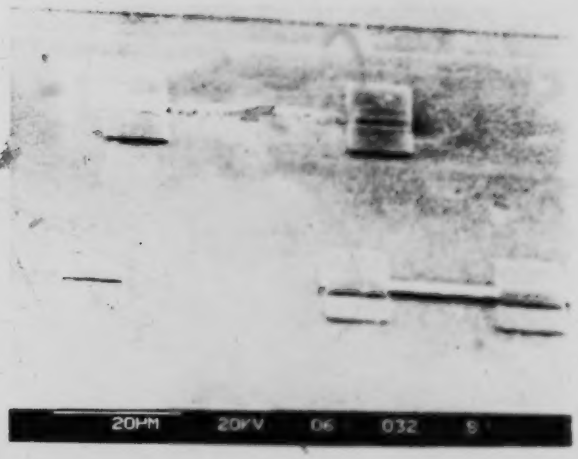


Figure 5.4. SEM photograph illustrating the effect of ion-implantation on polysilicon.

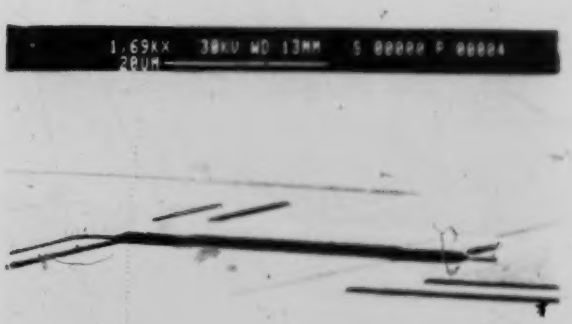


Figure 5.5. SEM photograph of a 10 μm x 70 μm polysilicon microbridge.

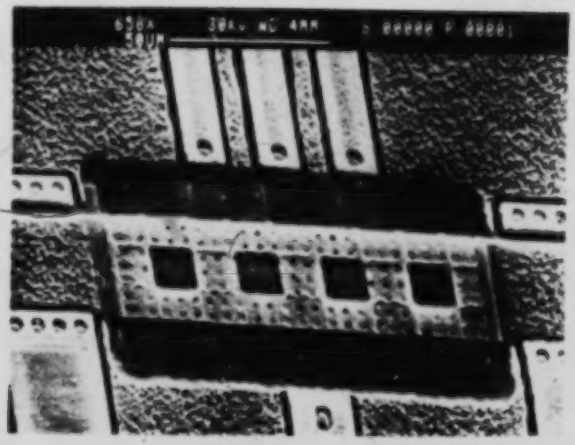


Figure 5.6. SEM photograph of a 30 μm x 100 μm polysilicon microbridge with apertures.

Figure 5.7. SEM photograph of a 10 μm x 120 μm collapsed microbridge.

6. OXIDE MICROSTRUCTURES

The second type of micromechanical devices that can be fabricated using the standard CMOS technology are oxide microstructures. This is apparent from the discussion presented in section 4.3 of this thesis. Careful analysis of the standard structures formed in CMOS technology suggests that microstructures based on the field oxide as a carrier (support) could be easily fabricated, if wet anisotropic etching of silicon is used as the final processing step. The two properties of anisotropic etching of silicon are extremely beneficial in this case, viz., the direction-controlled etch rate by the crystalline planes of silicon, and the selectivity by the etchant between silicon dioxide and silicon [14, 15]. Hence, the resulting pit formed in silicon by the appropriate photoprocess and anisotropic etching can leave a micromechanical structure of silicon dioxide on the top surface.

It is important to note that (100)-oriented silicon wafers are normally used in CMOS. In order to form a truncated pyramidal pit (or a pyramidal pit in some cases) in (100) silicon, a square opening has to be made in the oxide mask. The sides of the oxide mask opening have to be either parallel or perpendicular to the (110) edge of the silicon crystal (see Figure 6.1(a)) [14]. This particular edge will be indicated by the primary flat on any standard silicon wafer used for CMOS processing [1, 3]. The sides of the pyramidal pit formed by the anisotropic etching are the (111) planes of silicon. Figure 6.1(b) shows a SEM photograph of a (100) silicon wafer etched in EDP with rectangular openings in the oxide mask. In this photograph, we can distinguish the characteristic truncated pyramidal pits formed by the (111) planes of silicon. This is the result of the anisotropic etching process, where the etch rate in the direction of (111) planes is practically nil. If there is a misalignment of the edges of the mask with the (110) edge, then the anisotropic etchant undercuts the mask until the etchant meets the (111) planes [14, 15].

6.1 Oxide microbridge design in CMOS technology

The simplest method to fabricate an oxide microbridge is to form an oxide mask diagonally across a square opening of the kind illustrated in Figure 6.1(a). During anisotropic etching, due to the undercutting property of the etchant, an oxide microbridge will appear diagonally on top of the pyramidal pit. Since the standard CMOS processing technology uses (100) silicon and the placement of the layouts follows the so-called Manhattan pattern (either parallel or perpendicular to the primary flat) [1], the diagonal oxide layer defined by the layout can never be aligned to the (110) edge of the silicon wafer. This misalignment is necessary, in fact, for the anisotropic etchant to undercut the diagonal oxide layer to form the microbridge.

The sensor layout design for the oxide microbridge is shown in Figure 6.2(a). In order to expose a portion of the silicon substrate in two triangular shaped areas (on either side of the sandwiched oxide layer) to the anisotropic etchant, the sensor layout rule 3 is employed; described in section 2.3.3. An active area, contact-cut and pad-opening are placed one above the other in the areas where the silicon substrate has to be exposed. n+ and n-guard exclusion masks are defined in order to avoid any increase in the anisotropic etch time caused by the dopant concentration in silicon [14, 15]. Figure 6.2(b) shows the cross-sectional view of such a design implemented in standard CMOS technology.

6.2 Oxide cantilever design in CMOS technology

The sensor layout for the fabrication of a sandwiched oxide cantilever is shown in Figure 6.3(a). Here we exploit one of the properties of the silicon anisotropic etchant, namely its ability to undercut a convex corner. This process is the prevailing method for obtaining oxide cantilevers [14]. The layout design is such that the oxide layer which will form the cantilever structure produces the convex protrusion as shown in Figure 6.3(a). This layout implemented in the standard CMOS process will produce a structure whose cross-section is illustrated in Figure 6.3(b).

6.3 Post-processing for oxide microstructures

The post-processing step of anisotropic etching can be performed with EDP or KOH [14, 15]. As the oxide layers are not significantly attacked by the post-processing etchant, no additional masking step is required. However, since EDP's etch rate of silicon dioxide is much lower than that of KOH and KOH attacks aluminum bonding pads, the preferable etchant (for this postprocessing) is EDP. During this process, the etchant attacks silicon in those regions where the silicon substrate is exposed and the oxide microstructures form upon completion of the etching process. Note that the circuits formed by the CMOS process on the same chip is covered by the CVD oxide films. Since the CVD oxides are not attacked by the etchant, the circuits or other electrically functional devices formed underneath will be left as such. The characteristics of such devices are reported in section 6.7.

It has been reported that anisotropic etching with EDP attacked aluminum bonding pads, rendering them useless and preventing any further testing of the micromechanical device [14]. This effect was observed during the post-processing step initially. However, later it was determined that performing the EDP etching at a temperature between 95°C to 105°C left aluminum bonding pads unattacked. Hence, packaging and bonding of the devices were enabled for further electrical testing and characterization.

Figure 6.4 shows a SEM photograph of a 12 μm x 69 μm sandwiched oxide microbridge. In the SEM photograph of Figure 6.5, an oxide cantilever has a loop of polysilicon sandwiched between the field oxide and the CVD oxides. The dimensions of the cantilever are 24 μm x 205 μm.

6.4 Residual stress in oxide microstructures

It can be seen from Figure 6.5 that there is a slight upward curvature in the cantilever beam due to the residual stress in the oxide films. It is worth commenting at this point that this deformation is small considering the fact that the commercial CMOS process

is not actually meant for the fabrication of micromechanical structures. In fact, we found this curvature to vary little in all the samples on which we conducted the post-processing etching (120 dies).

6.5 Oxide microstructure functional devices

Using the oxide microstructure fabrication technique two functional devices were realised; a thermally isolated gas flow sensor, thermal and visible radiation source and an electrothermal microactuator. All the devices operate on the thermal behaviour of micromechanical structures, namely the thermal conduction through the oxide and surrounding ambient gas, incandescent light emission due to heating and the thermal expansion of silicon dioxide, respectively.

6.5.1 Thermally isolated gas flow sensor

Measurement and control of gas flow is important in many domestic and industrial applications. Usually, accurate measurement is determined from the cooling of a hot wire due to the gas flow [50]. In order to increase accuracy and portability and reduce power consumption, miniaturised gas flow sensors have been fabricated; recently silicon micromachining techniques have been used to fabricate such sensors [45, 49, 51, 52, 53, 54]. These micro-gas flow sensors were fabricated by a custom fabrication technology exclusively developed for this purpose. We have now demonstrated that similar gas flow sensors can be fabricated using the formalized approach with commercial CMOS technology.

6.5.1.1 Fabrication

To realise a miniature electrothermal gas flow sensor we require an electrical heater and a temperature sensor element placed in close proximity. This is done with two resistive elements sandwiched between two electrically insulating layers, such as SiO_2. When a current is passed through the heater, the temperature of the heater element increases, which can be observed by measuring the change in resistance of the sensor element. For a given current, a steady state temperature results; of the major heat loss mechanisms, conduction through the SiO_2 and the gas adjacent to the membrane is the most important for gas flow measurement.

The SiO_2 layers containing the two resistors are thermally isolated to reduce the heat conducted into the substrate [49, 52, 53]. The thermal isolation is achieved by silicon micromachining techniques [14, 15]. The importance of thermal isolation for gas flow measurement is demonstrated and discussed in section 6.5.1.4.2.

6.5.1.2 Sensor layout design for gas flow sensor

The sensor layout design which allows the formation of the basic structure required for the gas flow sensor is shown in Figure 6.6(a). This layout is designed using the sensor layout rule 3 (see section 2.3.3). Figure 6.6(b) shows the cross-section of the structure obtained after the CMOS process. The two resistive elements required for the gas flow sensor are formed using the polysilicon layer available in the CMOS process. One of the resistive elements, R_1 in Figure 6.6(a), is used as a heater element and the other, R_2, is used as the sensor element. The change in resistance of R_2 due to the change in heat flow from the heater to the sensor is used as the measure for detecting the gas flow.

6.5.1.3 Post-processing for gas flow sensor

To form the membrane structure, the post-processing procedure described in section 6.3 was performed. This process forms a rectangular membrane structure supported at the diagonal corners and suspended above the cavity formed by the anisotropic etching [14, 15]. This structure is shown in the SEM photograph of Figure 6.7; the resistive elements can be clearly seen.

6.5.1.4 Experiment

To evaluate the performance of the fabricated device the following characterization experiments were performed.

6.5.1.4.1 Determination of α_R of polysilicon

To use the device as a gas flow sensor, the temperature coefficient of resistance (α_R) of the CMOS polysilicon was determined by the following experiment. The device was placed in an oven and the temperature increased over the range 22 - 80°C. The resistance R of five similar polysilicon resistors was measured over this range and plotted, as shown in Figure 6.8. A least-squares fit of a straight line to each set of data yielded an average value for α_R of 1.17×10^{-3}/°C, with a standard deviation of 0.027×10^{-3} /°C. Since the chip holder used for the experiment could not be subjected to temperatures above 80°C, we could not directly measure α_R above this temperature. The validity of using the above value of α_R at temperatures greater than 80°C was verified indirectly, as described in the next section.

6.5.1.4.2 Electrothermal response

As a current I is passed through the resistor R_1, the value of the resistance R_2 will change as the thermally isolated oxide membrane and the polysilicon resistor R_2 heat up. The increase in temperature can be observed by the change in the resistance R_2, shown as curve (a) in Figure 6.9. The effective temperature (T) of R_2 may be obtained using the measured value of its resistance. The increase in T is calculated using the formula [50]

$$T = [(R(T)/R_0) - 1] / \alpha_R \qquad (6.1)$$

where: R(T) is the value of resistance R_2 at a temperature T,

R_0 is the value of resistance R_2 at 0°C and

T is the temperature in °C.

Two temperatures calculated in this manner are shown in Figure 6.11. The maximum temperature of R_2 was calculated to be 325 ± 9 °C for a power of 17.1 mW dissipated by the heater element.

Curve (b) of Figure 6.9 indicates the response obtained from a device that was not etched and therefore not thermally isolated from the substrate. This device underwent a calculated maximum temperature increase of only 87°C, due to heat conducted through the substrate, demonstrating the effect of thermal isolation.

To verify that the increase in temperature is proportional to the power dissipated in R_1, the value of $R_2(T)$ was plotted against $I^2 (1 + \alpha_R T)$. The plot is shown in Figure 6.10. The linear response observed from Figure 6.10 confirms that the increase in the temperature of R_2 is directly proportional to the power dissipated by the heater element. Figure 6.10 also indicates that the value of α_R obtained up to 80°C is valid up to 325°C.

and the higher order α_R components are negligible up to 325°C.

For the measurement of α_R the polysilicon was heated homogenously in the oven while the device during operation will produce an inhomogenous temperature distribution over the suspended plate. At high currents the nonuniformity may introduce significant error in the temperature estimate and other methods of temperature determination should be used. Determination of temperature profile using an infrared microscope is described in section 6.5.2.

6.5.1.4.3 Gas flow response measurements

To obtain optimum performance of the gas flow sensor, a laminar flow of the gas should be maintained parallel to the membrane. This achieves maximum heat transfer [46, 49, 50] to the gas and hence the largest change in resistance of the temperature sensor element. In the initial layout design phase of our gas flow sensor, provision for providing such laminar flow was not included, as we first wished to explore the feasibility of fabricating gas flow sensors using CMOS technology, before concentrating on refinements to be added in future.

To determine the potential performance of the device as a gas flow sensor, the membrane was exposed to a flow of helium from a nozzle placed near the sensor. The nozzle, of diameter 2 mm, was placed approximately 1 cm from the sensor, at a grazing angle. Two gas flow rates were used, and the measured values of R_2 under these gas flows are shown in Figure 6.11. Curve (a) is the no-flow case, curves (b) and (c) for the two calculated nozzle velocities of 5 and 12.5 m/s, respectively. At the maximum current of 4 mA in the heater element, we observe temperature decreases from the no-flow case of 78°C and 153°C.

These measurements do not allow the determination of the sensitivity of the device, as the flow velocities on the sensor are not known, nor is the nature of the flow (i.e.,

laminar or turbulent) over the membrane. Further improvement could be achieved by forming a channel, using silicon micromachining, to carry the gas directly over the sensor element [45, 49]. Such a channel could be readily obtained by the sensor layout design method in the CMOS process.

6.5.2 Thermal and visible radiation source

In the previous section the thermally isolated structure was used as a device for measuring gas flow. The temperature increase of the suspended plate structure due to the current flow suggests that this type of structure could be used as a pixel for *thermal resolution test targets*. Thermal resolution test targets are a matrix of point sources of thermal radiation (heat) used for calibrating infrared and thermal sensors [55]. Present day miniature incandescent light sources and thermal resolution test targets are fabricated using customized fabrication technologies [55, 56].

6.5.2.1 Thermal radiation source

The thermally isolated structure demonstrated in the previous section is ideally suited for application involving thermal radiation sources. To evaluate the temperature distribution over the suspended plate when a steady current was passed through the heater element, several thermal maps were obtained using an infrared microscope. The thermal mapping was performed at National Institute of Standards and Technology (NIST), Gaithersburg, Maryland, USA. The emissivity ϵ of the thermally isolated structure, and the polysilicon element in particular, is first determined by the following procedure. First the infrared microscope was initialized by a blackbody kept at a known, constant temperature. Then the device under test, maintained at the same temperature as the black body, is brought under the microscope and the relative decrease in the amplitude of the emitted energy is calculated. Computing the ratio of the energy between the blackbody and the device, the emissivity ϵ can be readily calculated. The ϵ obtained in this manner for the

device under test was 0.4 [79]. A typical thermal map is shown in Figure 6.12. This map was produced for a current of 3 mA through the heater element. It can be seen that the maximum temperature is 170°C. The 130°C isothermal line passes through most of the polysilicon resistor element adjacent to the heater element. For the same current, the calculated temperature is 128°C; this temperature is indicated on the graph of Figure 6.9 at the appropriate current.

The thermal mapping has verified that the thermally isolated structure can indeed function as a thermal radiation source. At the same time it confirmed that the temperature calculated using eqn. (6.1), although an indirect method, is quite close to the actual experimental measurements.

6.5.2.2 Visible radiation source

From the electrothermal response reported in section 6.5.1.4.2, it can be seen that the temperature can go as high as 325°C for an input current of 4 mA. The device remains functional for currents higher than 4 mA, producing higher and higher temperatures and eventually reaching the incandescent point. This occurs at 4.9 mA, and the visible radiation can be clearly seen emitting from the chip surface.

A systematic experiment was performed to study this effect and an I-V plot was made to study the incandescent effect more systematically; a typical curve is shown in Figure 6.13. Here we can see a discontinuity in the slope at 5.2 mA (point d1), which could be due to an avalanche breakdown effect in polysilicon [56]. However, we suspect that due to the high temperature, oxygen diffusion through the oxides, especially the top CVD oxides, can oxidize the CMOS poly and cause this change. Hence, another I-V measurement was performed with the chip placed inside a nitrogen-filled chamber. The results are indicated by curve (b) in Figure 6.13 In this case, the abrupt change in the slope occurs at 5.7 mA (point d2) and the device remains functional up to 7.1 mA.

The optical radiation output was measured at NIST by placing the device 30 cm from a 1 cm^2 calibrated silicon photodetector sensitive to radiation below λ = 1.25 μm. Typical results are shown in Figure 6.14. At a current of 6.1 mA (35 mW of input electrical power), the integrated intensity was measured to be 8.2 x 10^{12} photons/second/steradian. Using an optical microscope, it was determined that only 70% of the area of the poly was emitting visible radiation. Using this figure and the intensity obtained, the emittance was calculated to be 1.9 x 10^{22} photons/m^2. Comparing this value with that of a blackbody, the emittance over the incandescent portion of the poly corresponds to a temperature of 1400K.

From Figure 6.13 we observe that visible radiation is obtained from the micromachined CMOS device below the slope discontinuity in the I-V characteristics (point d1). Thus the device can be used as an optical source in this region. If operated beyond the slope discontinuity (point d1) an irrecoverable shift in the I-V characteristics results, as indicated by curve (c). This might be due to the annealing of the poly by the heat generated during the current flow. Another explanation could be doping of the poly with phosphorous from the top CVD oxide [42].

6.5.2.3 Long term effect and drift characteristics

In order to determine the drift characteristics of the thermally isolated poly resistor a lifetime experiment was performed. A set of poly elements were chosen and subjected to various levels of continuous current. The zero-current resistance were monitored against time. Over a period of 150 hours, poly elements subjected to continuous current of 4.5 mA exhibited a 60% increase in the resistance, elements subjected to 4 mA a 40% increase and elements subjected to 3 and 3.5 mA a mere 1% increase in the resistance. These long term drift characteristics are shown in Figure 6.15. The increase in the resistance could be due to oxidation of the poly, which would reduce the cross-sectional area and hence increase the electrical resistance. Another possible reason could be due to electromigration of the polysilicon. Electromigration of aluminum is one of the major failure mechanism in VLSI

chips [1] and similar electromigration effects could be present in polysilicon lines. This effect could contribute to the gradual increase of the resistance of the poly element. More detailed investigative experiments are necessary to confirm this possibility.

Although the resistance of the poly element exhibits a considerable amount of drift at the visible radiation level, the drift exhibited at lower temperatures is very small and shows that this device can be ideally suited for thermal resolution test targets, where a temperature increase of only 300°C above the ambient is needed [55].

6.5.2.4 Calculation of visible radiation efficiency

Assuming all the input power is converted to blackbody radiation, the equivalent black body temperature can be calculated using the Stefan-Boltzmann radiation law;

$$E = \epsilon \, \sigma \, (T^4 - T_o^4) \qquad (6.2)$$

where: E is the energy radiated per unit area

ϵ is the emissivity

σ is Stefan's constant

T is the equivalent blackbody temperature in Kelvin and

T_o is the ambient temperature in Kelvin.

Substituting 35 mW over the poly area of 1908 μm^2 as E in equation (6.2), we obtain an equivalent blackbody temperature T of 5333K. This is too high a value, but is expected because our assumption ignores possible heat losses. Since a considerable amount of heat is conducted through the poly, oxide and the ambient air by conduction and convection, only a fraction of the input power is converted to radiation.

The temperature estimate over the incandescent area of the poly described in section 6.5.2.2 gives an equivalent blackbody temperature of 1400K. Using this temperature, the

equivalent energy radiated is 0.165 mW. Comparing this power with the input power of 35 mW, the radiation efficiency is 0.5%. The radiation efficiency can presumably be increased by placing the device in vacuum to reduce the heat loss due to convection. However the heat loss due to conduction through the oxide cannot be eliminated and hence, any significant increase in the efficiency cannot be expected.

The micromachined visible radiation source in its present form is not comparable with that of the micro-incandescent lamp fabricated by Masterangelo *et. al.*, [56]. This is due to different processing and packaging techniques employed in their fabrication approach.

6.5.3 Microactuators

Microactuators represent one of the key components for potential future applications ranging from micro-robots [33, 36, 57] to miniaturized scanning tunnelling microscopes [58]. In general, the mechanical deflection of microelectronic devices is usually associated with the piezoelectric effect. Materials such as ZnO and quartz crystals are commonly used because of this piezoelectric effect and are fabricated into various types of transducers, especially actuators. Present day microelectronics makes extensive use of silicon for the fabrication of circuits as well as sensors. Unfortunately, silicon does not exhibit piezoelectric behaviour which could be used to fabricate microactuators. Silicon and its compounds however, do exhibit a wide range of coefficients of thermal expansion that could be effectively used to fabricate microactuators.

6.5.3.1 Electro-thermal actuators

One of the earliest actuators used for temperature control applications is the bimetal thermostat [59]. In this type of thermostat, two metals of different coefficients of thermal expansion are attached together to form a bimetal strip. This strip, when subjected to a temperature increase, curls towards the metal with the lower coefficient of thermal

expansion and produces a mechanical deflection. The differential thermal expansion effect was recently explored in the fabrication of silicon microactuators by Riethmuller *et al.*, [60]. Two thermally conducting layers (p^+-Si and Au) and an electrically isolated heating resistor were used to fabricate a cantilever microactuator. The effect of differential thermal expansion of the P^+-Si and Au layers is used to produce the mechanical deflection. The above-mentioned microactuator is fabricated using a customized process. In the following sections, fabrication, testing and performance of a similar cantilever-type CMOS microactuator is described.

6.5.3.2 CMOS microactuator fabrication

In order to produce a functional microactuator, a sandwiched oxide cantilever should be fabricated using the standardized approach. The sensor layout required for obtaining the basic structure in CMOS process is described in section 6.2. Here, the sandwich structure is formed out of field oxide (thermal oxide), polysilicon and the phosphorous doped CVD oxide. The cross-sectional structure is shown in Figure 6.3(b). The sandwiched polysilicon functions as a heater that is required to raise the temperature of the sandwich structure for the microactuator action. The post-processing step required to form the free standing cantilever is described in section 6.3

6.5.3.3 Experimental testing and discussion

The performance of the cantilever microactuator was evaluated by conducting amplitude and frequency response experiments.

6.5.3.3.1 Amplitude response

To evaluate the amplitude response of the microactuators, a dc current was passed through the polysilicon heater and the mechanical deflection was observed and measured using an optical microscope. The movement of the microscope in keeping the deflected

microactuator in focus indicated the deflection. The accuracy of measuring deflections using the optical microscope in this manner was estimated at 20%.

The field oxide, which forms the bottom layer of the structure, is grown thermally; the insulation layers which follow (CVD oxides) are grown by the LPCVD process [1]. Due to the difference in the field oxide and CVD oxides growth processes, different packing densities would result and hence a different coefficient of thermal expansion. The differing coefficients of thermal expansion were observed as a deflection of the free end of the cantilever above the substrate when a current is passed through the heater element. Typical response is shown in Figure 6.16. The microactuator exhibited an elastic deflection up to 4 μm above the chip surface as a function of input power. Input powers exceeding 5.6 mW produced irrecoverable plastic deformation. This effect could be possibly due to the excessive amount of heat generated by the heater which anneals the oxides and generates permanent strain. The SEM photograph shown in Figure 6.17 shows one such plastically deformed cantilever.

Following the theory outlined in [59, 60], one of the basic parameters to describe the behaviour of a cantilever microactuator is the conversion factor γ_E, which relates the deflection of the free end of the cantilever to the input electrical power. Computation of γ_E analytically is very difficult but can be determined experimentally using the relation [60]:

$$\partial = \gamma_E P_i \qquad (6.3)$$

where: ∂ is the deflection

P_i is the input electrical power.

In computing γ_E for the cantilever microactuator, the deflection was plotted against input electrical powers between 2 mW and 5.6 mW (see Figure 6.18). The slope of the response shown in Figure 6.18, γ_E, is calculated to be 0.97 μm/mW.

6.5.3.3.2 Frequency response

To determine the frequency response of the microactuator, a square wave signal, with 50% duty cycle, and frequency varying from 1Hz to 10kHz was applied to the heater element. The square wave produced an oscillation of the cantilever. Using the microscope, the extreme positions of the tip of the cantilever was measured as a function of frequency. Typical response is shown in Figure 6.19. At low frequencies the heating and cooling of the oxide sandwich takes place slowly enough and the deflection can follow the input signal, as indicated by the area marked *oscillating region* of the Figure 6.19. When the frequency is increased the amplitude swing decreases until it reaches a constant value at 1.5 kHz. This effect could be due to the inability of the cantilever structure to cool completely between heating cycles. Hence, the microactuator is unable to follow the input signal and produces a constant deflection above 1.5 kHz.

6.5.3.3.3. Analysis of microactuators

The commercial semiconductor fabrication industry does not reveal process parameters such as the thicknesses of various oxides and the exact composition. Therefore, at this stage, a full theoretical analysis of the microactuators based on a commercial IC process is difficult. However, an approximate theoretical analysis can be performed using the available parameters for comparative study with the experimental results. In order to do this, initially the temperature increase, ΔT, was calculated using a thermal model and determined to be 31°C. (The details of thermal modeling is described in chapter 7 and the calculation of ΔT is detailed in Appendix B). The deflection exhibited by the microactuator is linearly approximated and illustrated in Figure 6.20. From Figure 6.20, the effective deflection δ for the analysis was calculated to be 2.2 μm. Using the formula for deflection of bimetallic strips [59]

$$1/s = (3/2)\,(\Delta\alpha_T/h)\,(\Delta T) \qquad (6.4)$$

and $$\partial = L^2 / (8s) \qquad (6.5)$$

where: s is the radius of curvature of the deflected bimetal strip

$\Delta\alpha_T$ is the differential thermal expansion coefficient of the sandwich material,

h is the total thickness of the sandwich and

L is the effective length.

$\Delta\alpha_T$ can be calculated to be 5.5×10^{-5} /°C.

To approximately determine the theoretical limit of the frequency of oscillation of the cantilever microactuator the solution of Fick's Second Law appropriate for (heat) diffusion in one dimension from a thin planar source into a semi-infinite solid can be used [80]. This relation is given by the expression

$$C(x, t) = C_o \exp(-x^2 / 4 D t) \qquad (6.6)$$

where: C(x, t) is the concentration of a diffusing species at a distance x and time t

Co is a constant and

D is the diffusion coefficient.

For the cantilever not to exhibit any response to the input ac signal, the heat generated by the poly should be completely contained inside the cantilever material itself. Hence, the time taken for the heat to travel from the poly to the boundary of the cantilever can be used as a measure of the minimum period of the ac signal. This time can be derived from equation (6.6) by equating $C(x, t)/C_o$ to 1/e; the period t can be expressed as

$$t = x^2 / 4 D \qquad (6.7)$$

where: $D = \kappa / c \rho$ and

κ is the thermal conductivity of the oxide

c is the specific heat capacity of the oxide and

ρ is the mass density of the oxide.

Substituting the values $\kappa = 0.011$ W/cm °C, $c = 670$ J / kg °C, $x = 1$ μm and $\rho = 0.26$ kg / cm^3, the period is calculated to be 3.9×10^{-5} seconds, corresponding to a maximum frequency of 25.2 kHz.

This theoretically computed frequency limit is much higher than the experimentally observed value of 1.5 kHz. The difference could be due to two reasons. Firstly, the simplified assumptions made for the analysis accounts only for heat travel in the vertical direction. The lateral diffusion of the heat to the edges of the cantilever is ignored. If we account for the lateral diffusion of the heat to the edges, the effective distance x would increase and would result in an increased period. This would reduce the calculated frequency. Secondly, the optical method of determining frequency relies on the visual determination of the oscillation of the beam and the depth of focus of the microscope. This method could introduce significant errors in the measurement of frequency of oscillation. Further, the dynamic mechanical properties of the CMOS oxides are not available and hence, the influence on the oscillation of the electrothermal actuator cannot be determined at this time.

To understand and formulate the exact functioning of CMOS electro-thermal microactuators, a more systematic experimental study of different types of actuator geometries, and measurement of deflections using laser interferometric systems [61] rather than an optical microscope is necessary. Interaction with the IC fabrication industry and obtaining relevant parameters such as thicknesses of various process layers and electrical and mechanical parameters is absolutely essential. Fortunately, electrical parameters of process layers used in the IC process are usually available [5]. However, it will be necessary to determine most mechanical and thermal parameters using experimental

methods.

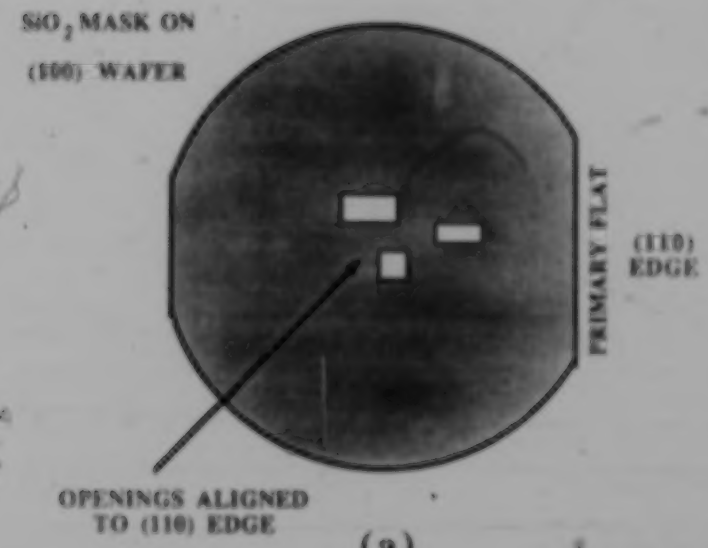
6.6 Design portability

Although most of the microstructure fabrication techniques reported in this thesis were based on the CMOS processes offered by Northern Telecom Ltd., [5], using the same layout design technique and post-processing, micromechanical structures could be fabricated using any standard industrial IC process [6, 7]. This is due to the fact that commercial CMOS IC fabrication processes available throughout the world are almost identical. Minor changes in the process do exist which are unique to the company that offers the IC process. However, micromechanical structures fabricated through those IC processes using the regularized approach do not show any noticeable difference. This was confirmed using SEM photographs of the various micromechanical devices fabricated using different processes. This aspect, called design portability between processes, is crucial to the industries to develop commercial micromechanical sensor and actuator systems using any available commercial IC technologies. The companies other than Northern Telecom, whose IC processes were used for testing the design portability concept are the Faselec Corporation, Zurich, Switzerland [7] and MOSIS [6], a commercial IC fabrication source in California, USA.

6.7 On-chip circuit integration

One of the advantages of the approach reported in this thesis is the ease of integration of on-chip electronics for the sensors or actuators. Although this on-chip integration of support electronics was demonstrated for the CMOS humidity sensors, conceiving proper circuits for the micromechanical devices became very difficult. This was due to the unavailability of the full physical, mechanical, electrical and thermal parameters for the CMOS process-layers. Also, there are no reported figures for CMOS fabricated micromechanical structures, since this research describes for the first time the fabrication of

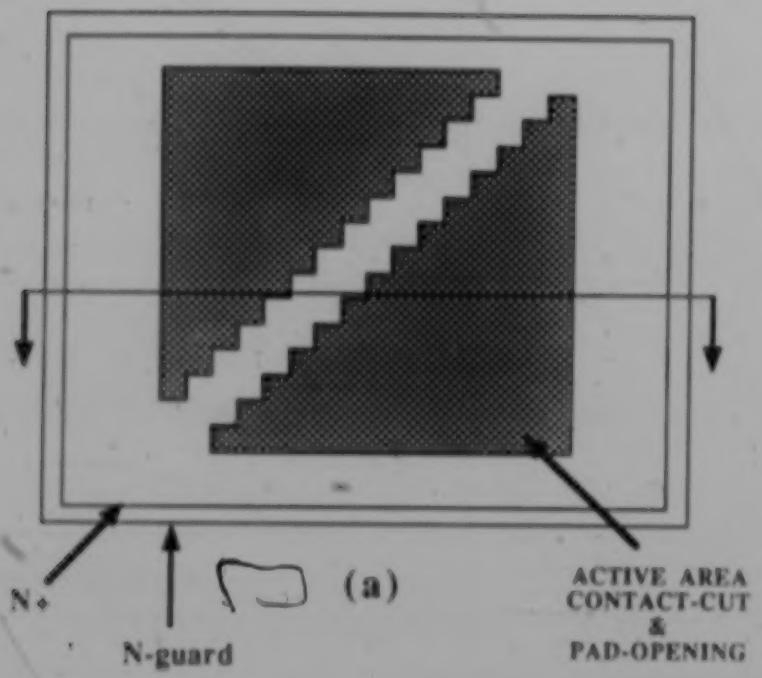
micromechanical structures using commercial CMOS processes. In order to test the on-chip integration concept, standard layout designs for several transistors were included along with the sensor layout design. The characteristics of these tramistors were measured before and after the post-processing step and were found to be identical. Typical results are shown in Figure 6.21 and 6.22. This experimental verification confirms that a circuit integrated with the sensor structure will remain functional and can form the on-chip support electronics for micromechanical sensor or actuator system.



(a)

(b)

Figure 6.1. Illustration of oxide mask alignment on a (100) silicon wafer.



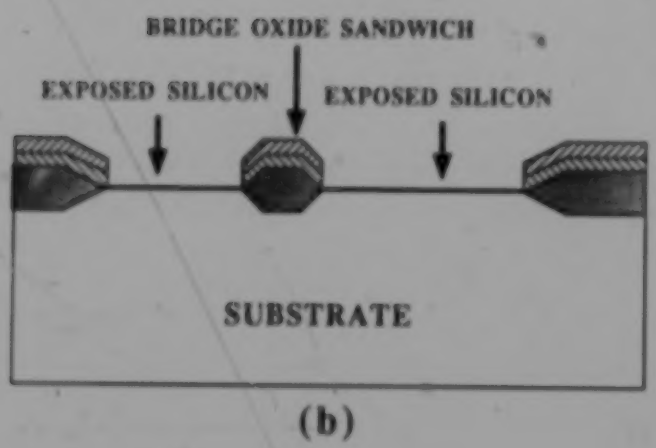


Figure 6.2. Sensor layout design for the fabrication of the sandwiched oxide microbridge in CMOS technology. (a) Layout view (b) Cross-sectional view.

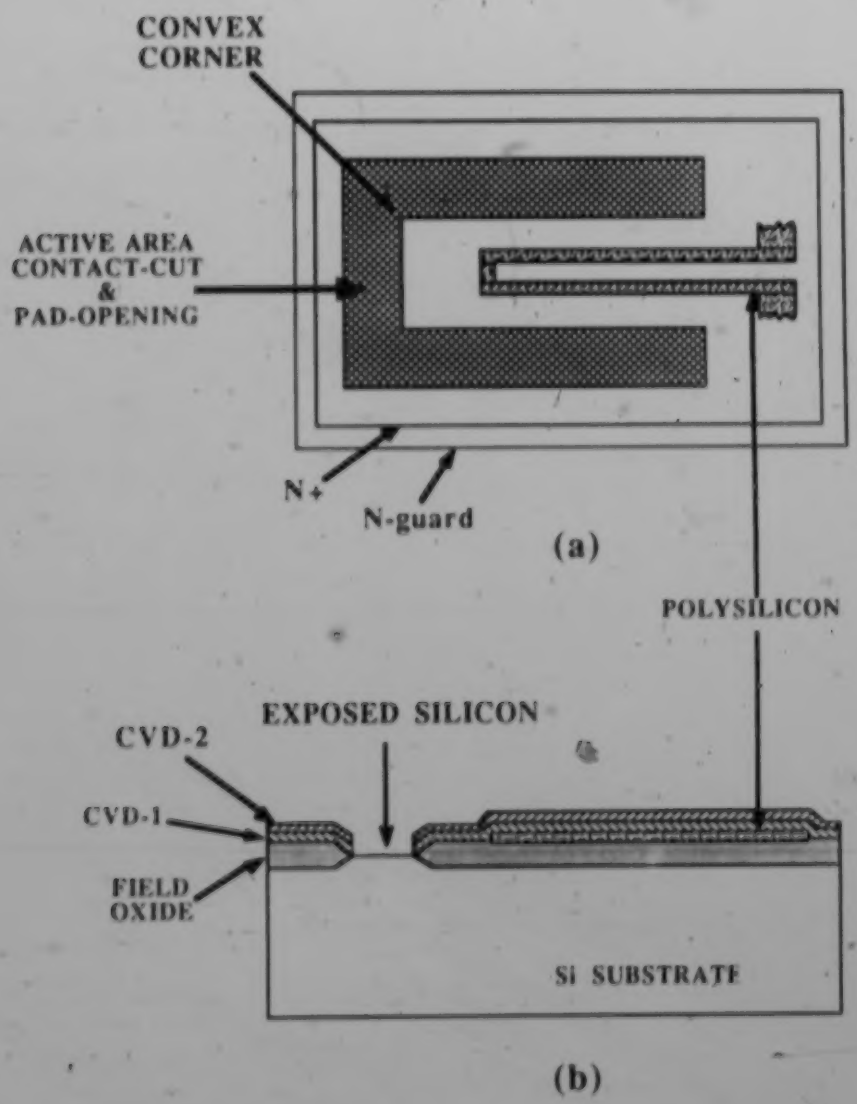


Figure 6.3. Sensor layout design for the fabrication of the sandwiched oxide cantilever in CMOS technology. (a) Layout view (b) Cross-sectional view.

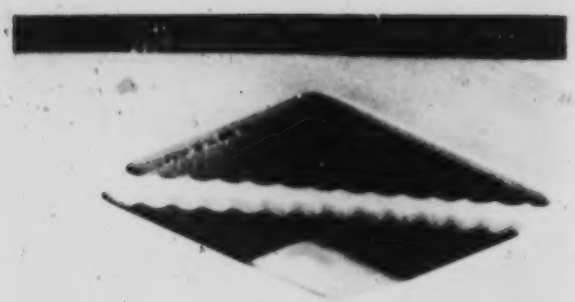


Figure 6.4. SEM photograph of a 12 µm x 69 µm sandwiched oxide microbridge.

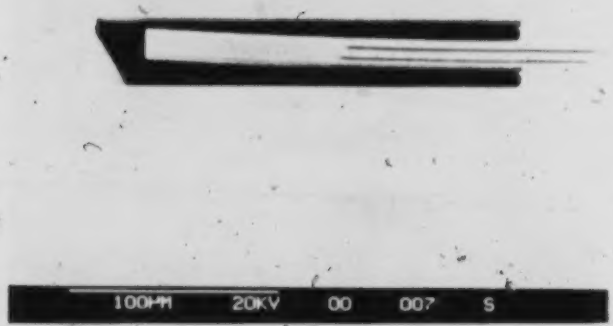
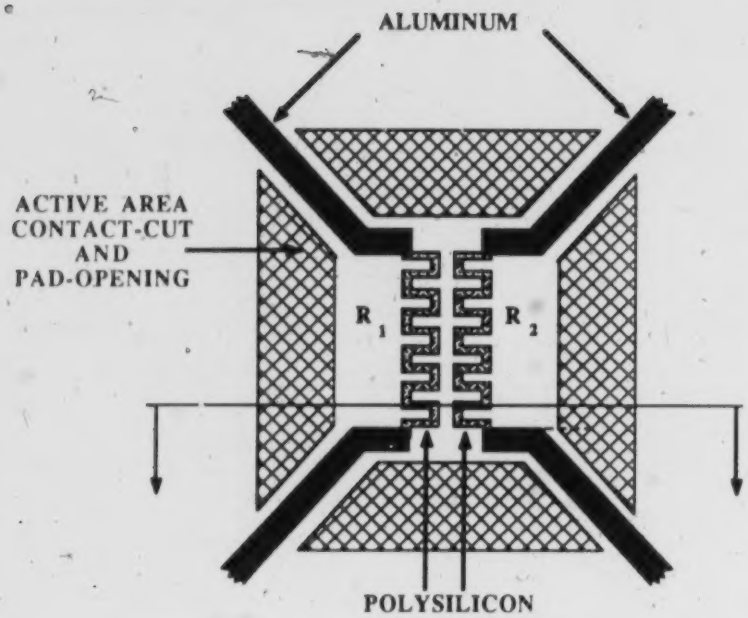
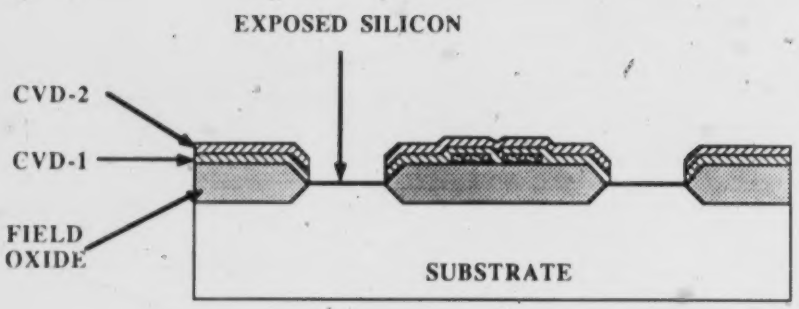


Figure 6.5. SEM photograph of a 24 µm x 205 µm sandwiched oxide cantilever.



(a)



(b)

Figure 6.6. Sensor layout for the fabrication of a thermally isolated structure with two poly-resistors. (a) Layout view (b) Cross-sectional view.

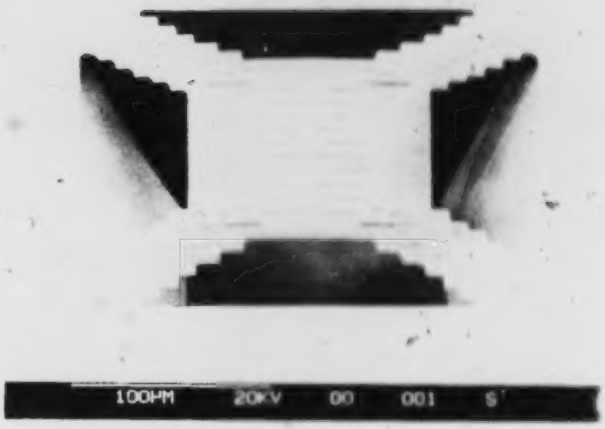


Figure 6.7. SEM photograph of the completed thermally isolated structure.

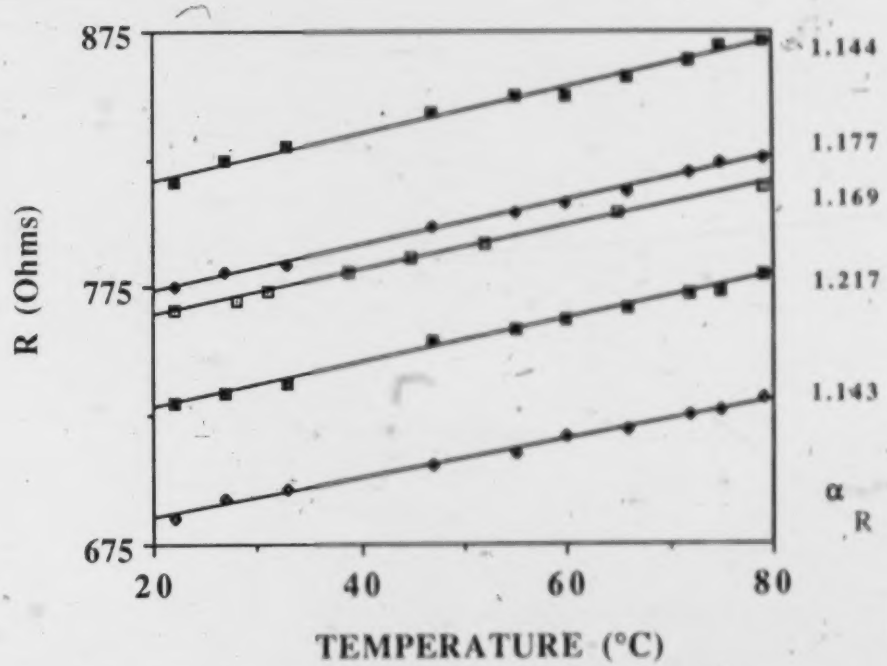


Figure 6.8. Variation of the resistance of the poly-resistors with temperature.

α_R Units: 10^{-3}/°C

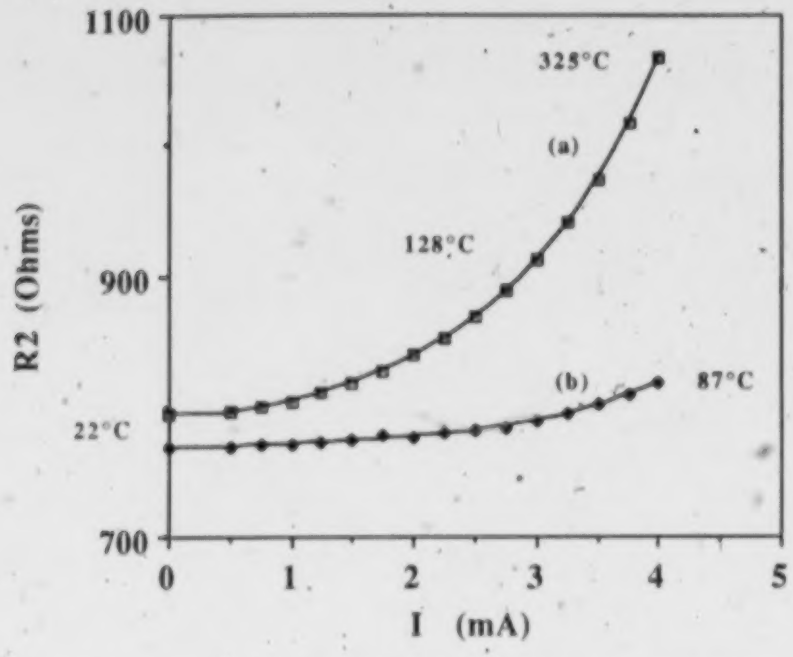


Figure 6.9. Electro-thermal response of the thermally isolated device.

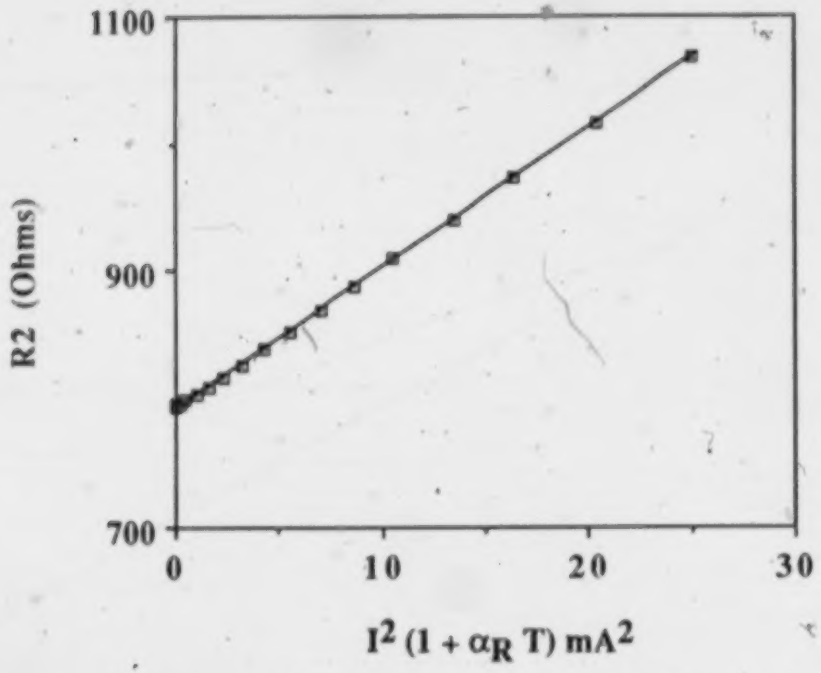


Figure 6.10. Variation of resistance with $I^2 (1+\alpha_R T)$.

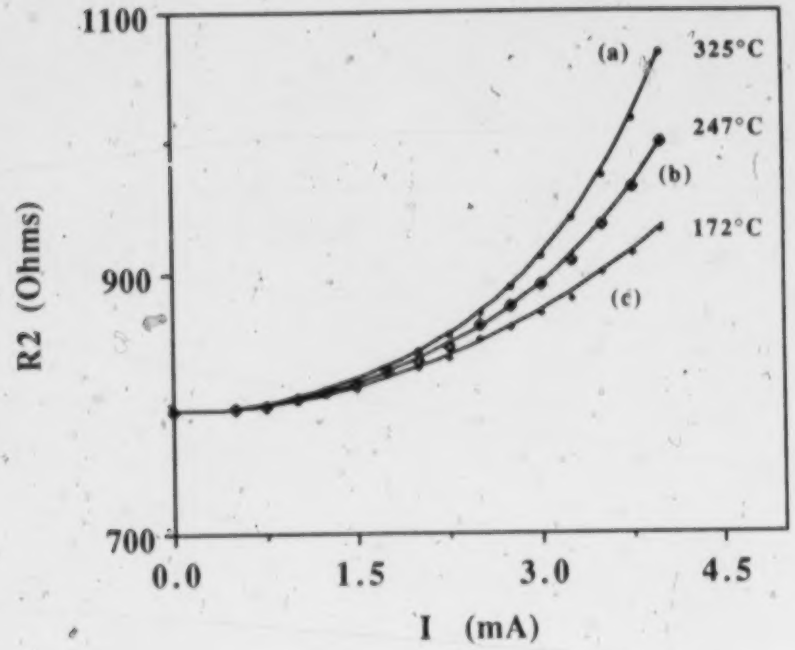


Figure 6.11. Gas flow response. (a) no flow, (b) 5 m/s and (c) 12.5 m/s.

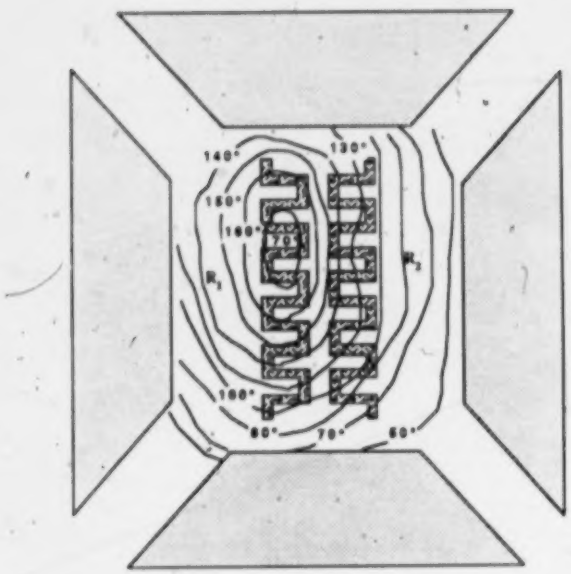


Figure 6.12. Thermal map of the CMOS thermally isolated device for 3 mA input current.

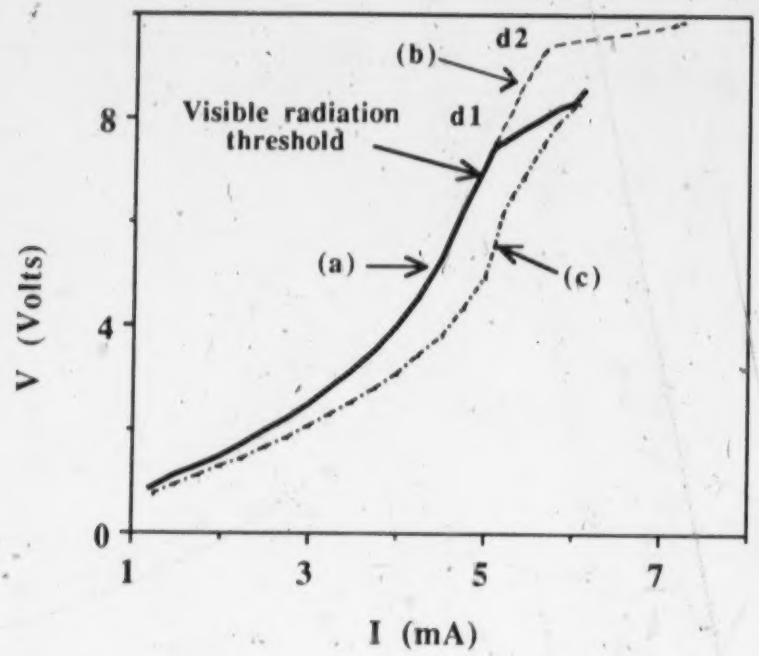


Figure 6.13. I-V characteristics of the thermally isolated poly resistor.

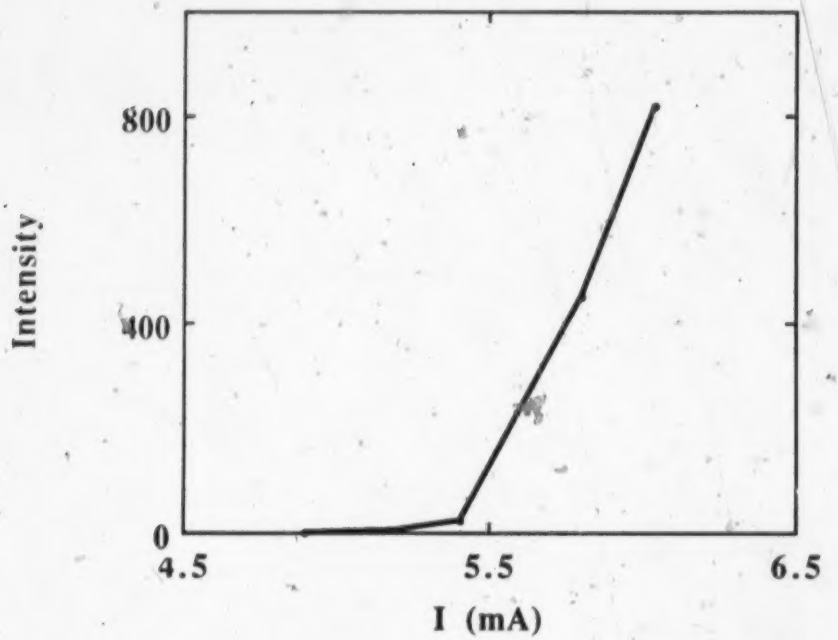


Figure 6.14. Visible radiation output characteristics.

Intensity units: 10^{10} Photons/second/steradian.

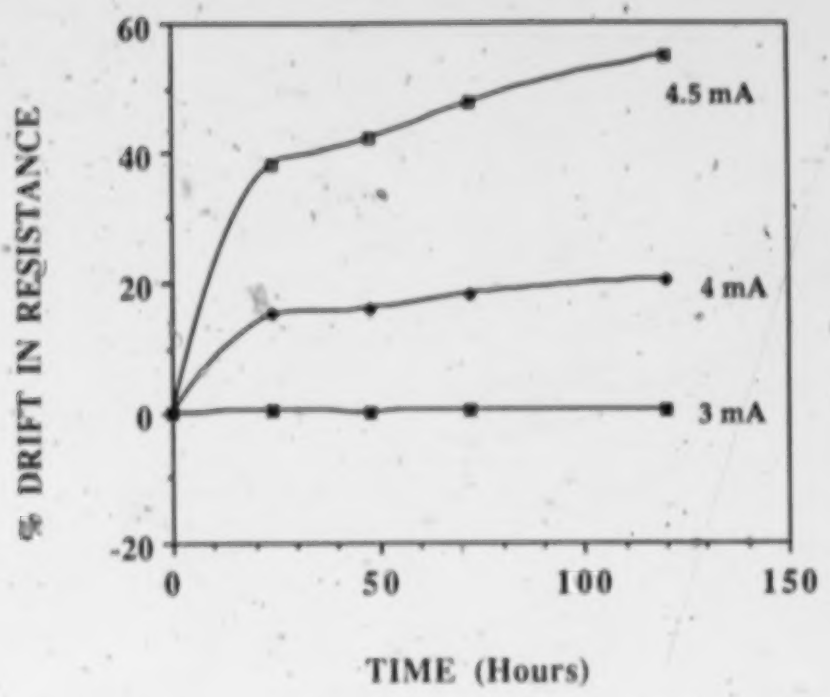


Figure 6.15. Long term drift characteristics of the polysilicon elements.

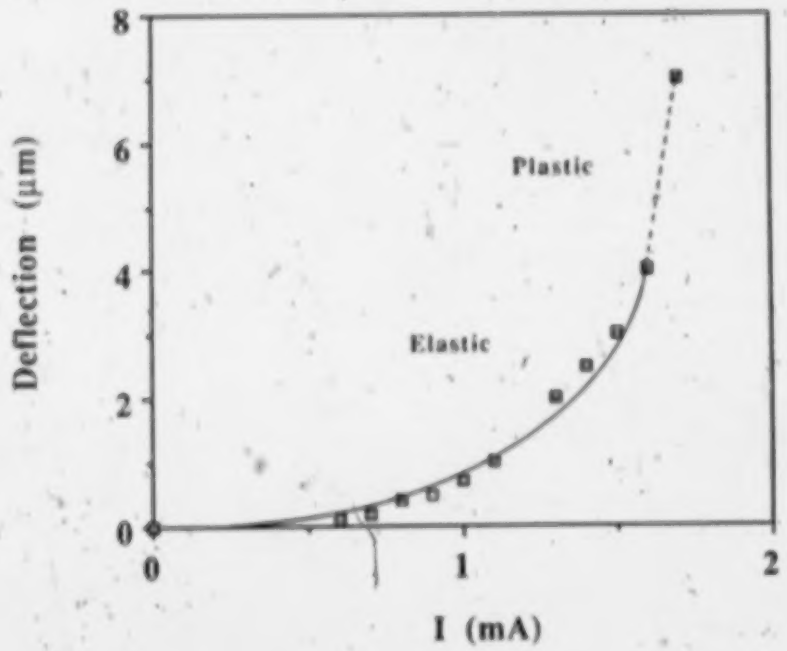


Figure 6.16. Amplitude response of the cantilever microactuator.

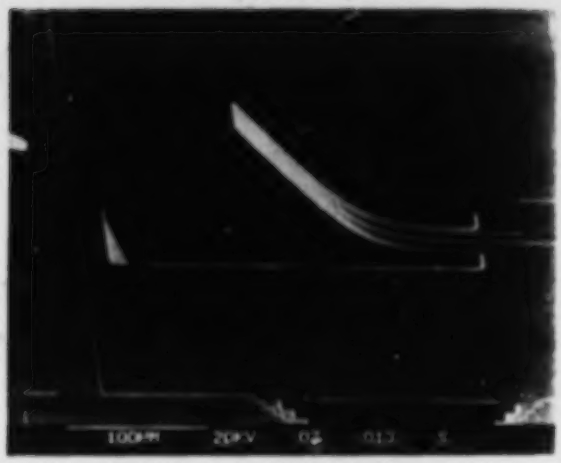


Figure 6.17. SEM photograph of a plastically deformed cantilever microactuator.

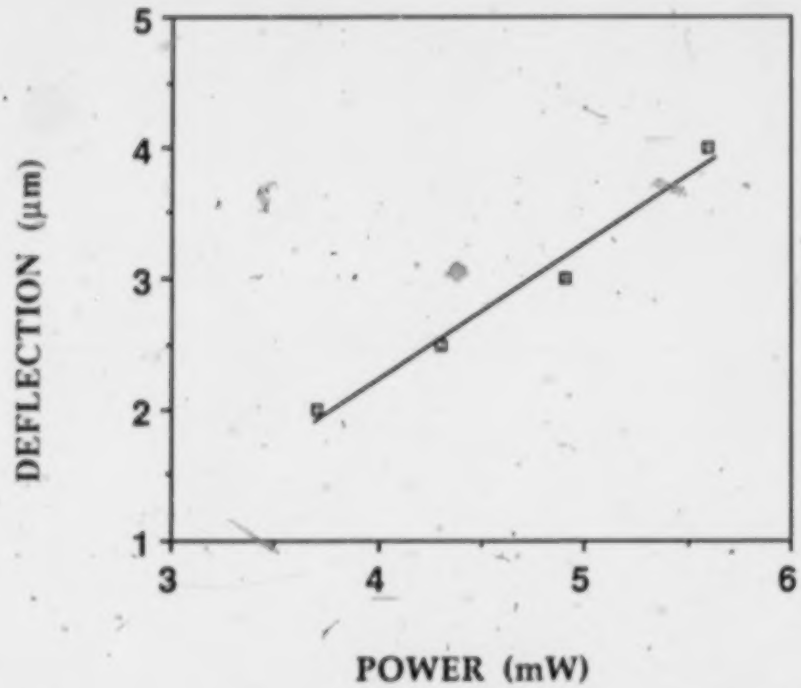


Figure 6.18. Amplitude response of the cantilever microactuator with respect to input electrical power.

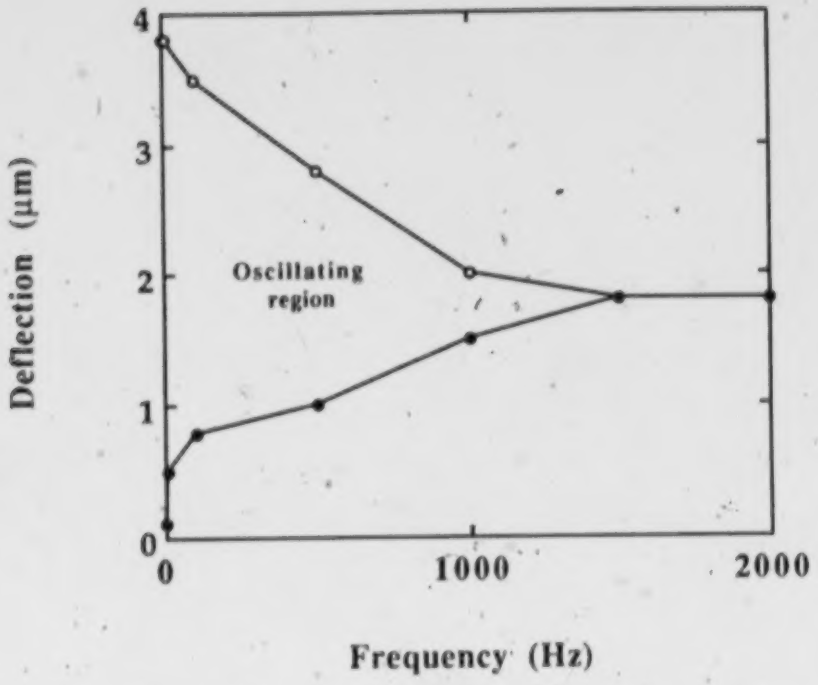


Figure 6.19. Frequency response of the cantilever microactuator.

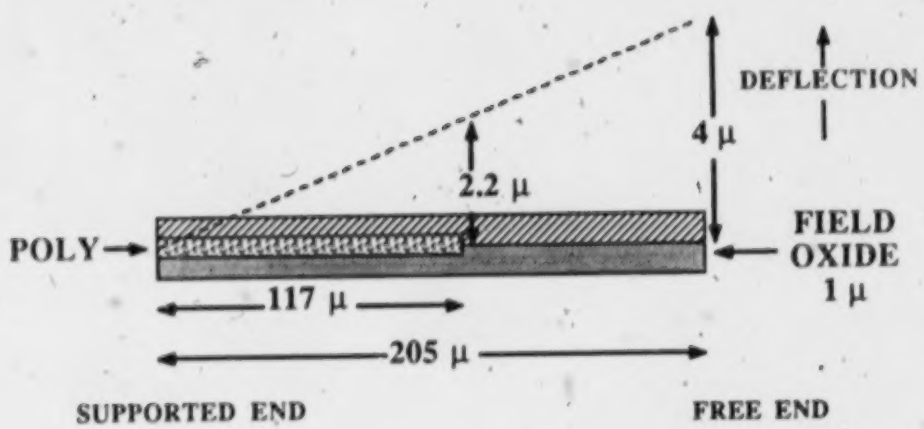
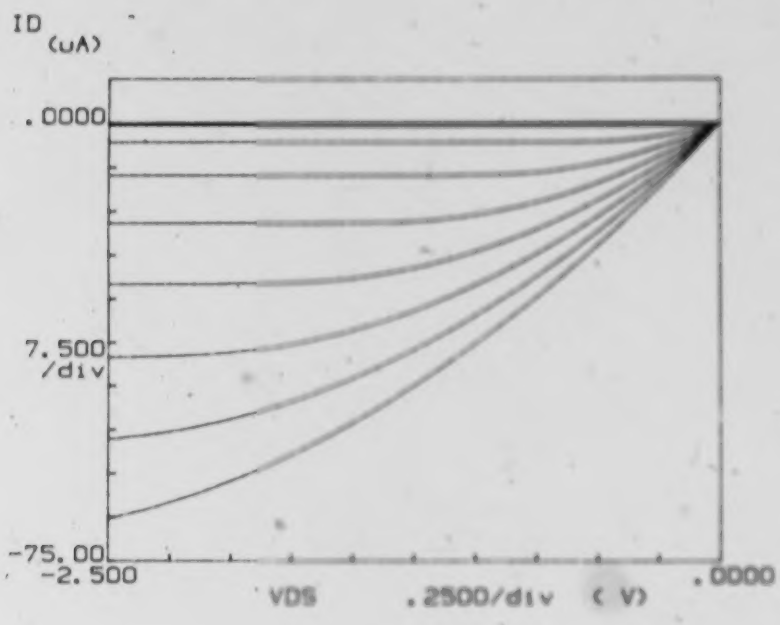
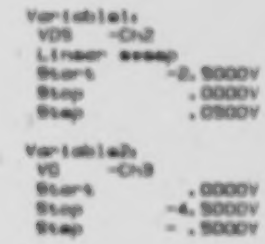


Figure 6.20. Linear approximation of the deflection of the cantilever microactuator.

(a)





(b)

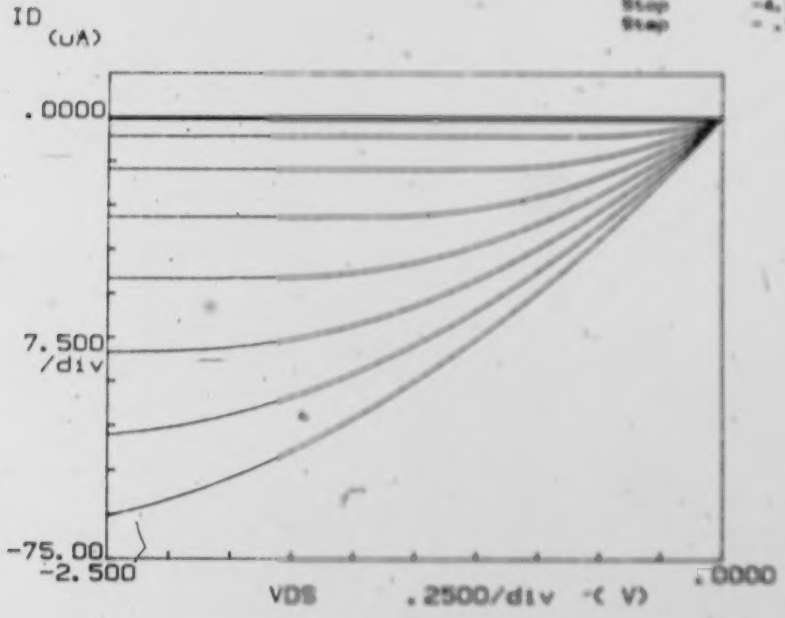
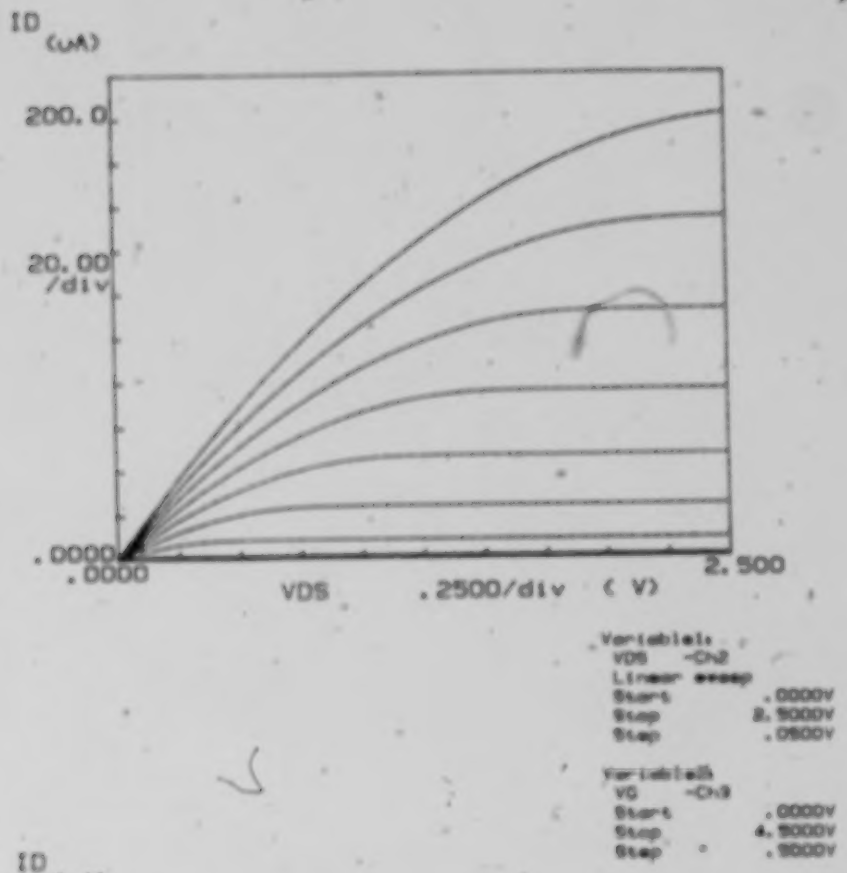
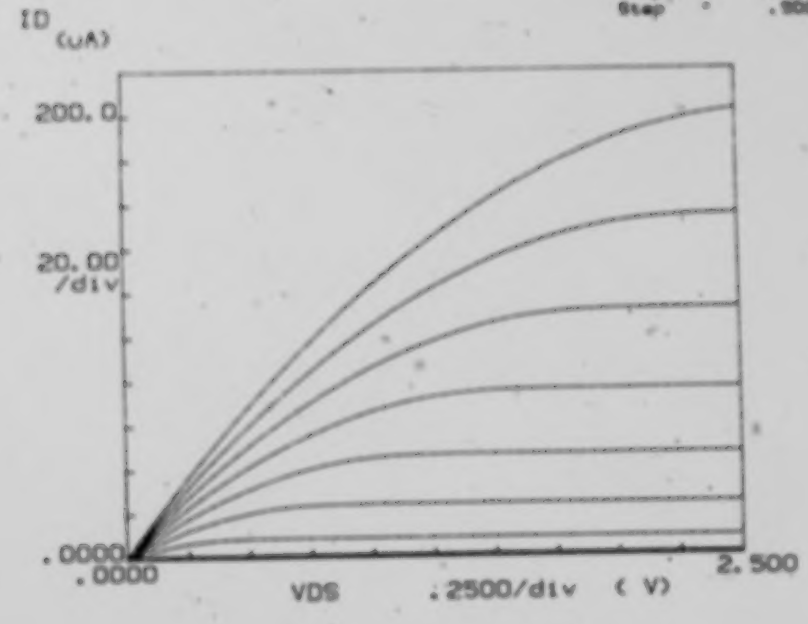


Figure 6.21. Characteristics of MOS transistors - P-type.

(a) before EDP etching (b) after etching.



(a)



(b)

Figure 6.22. Characteristics of MOS transistors- N-type.

(a) before EDP etching (b) after etching.

7. SENSOR MODELING

The goal of modeling is to produce a representation or simulation of a problem or process [62, 63]. In some cases, a description or analogy is used to help visualize the underlying process that cannot be directly observed. Modeling provides insight into the functioning and performance aspects of the device under study and quantitative evaluation of their performance becomes possible. It is especially valuable for the determination of various device parameters that are beyond the reach of experimental techniques. More importantly, modeling can be used to provide information to the user for optimum device performance. The process of developing microelectronic sensor systems involves several design trials as well as fabrication and testing cycles in order to obtain satisfactory results. These stages are often time-consuming and expensive, especially when a novel idea is to be implemented. In this sense, the concept of modeling provides a good alternative for the designers and the inventors. With the use of modern powerful computers, complex and exhaustive computations can be performed with relative ease. Since all these situations are invariably encountered, modeling proves to be a valuable tool for sensor research.

7.1 Analytical and numerical modeling

The approach employed in modeling usually involves the development of a suitable model with appropriate boundary conditions. In general, there are two types of modeling in use today, namely *analytical* and *numerical* modeling [63]. In analytical or regional modeling, crude simplifying assumptions are employed on both device geometry and the mathematical model [63]. Devices are usually treated as one-dimensional structures in this approach. Often the approach turns out to be unsuitable in many cases due to its dependency on the simplifying assumptions. However, analytical modeling has the advantage of providing a means for a better understanding on the functioning of a sensor. Hence, it often serves as a first step towards analysing the functioning of a new type of sensor.

Numerical modeling on the other hand, provides a more accurate estimation of the functioning of a sensor. It can serve as an aid for a deeper understanding of device behaviour and as a predictive design tool for the optimization of the device performance.

7.2 Microsensor modeling - mechanical effects

The most recent interest in the area of sensor modeling is in the micromechanical and thermal effects of microelectronic sensors. The earliest numerical package developed for micromechanical structure modeling was SENSIM [64]. This package is based on a two-dimensional finite difference code, which solves a system of partial differential equations that govern the stress resultants and deflection in a diaphragm. SENSIM is valid only for quasi-static, plane stress, isothermal and small deflection conditions [64]. A variety of other packages have been employed to simulate diaphragms and cantilever accelerometers to extract values of pertinent mechanical parameters such as Young's modulus, bulk modulus and Poisson's ratio [65-70]. Finite element numerical simulation packages are also being developed taking into account structural inhomogenieties and thermal effects [71, 72].

7.3 Thermal effects

Modeling and simulating thermal effects in semiconductor devices is in general well established [62]. Modeling the thermal effects in contacts and vias have also been established recently [73, 74]. Modeling thermal effects in sensors, specifically in micromechanical structures is, however, only at its infancy [53, 75-77]. Numerous micromechanical devices such as thermally isolated gas flow sensors, electrothermal microactuators and membrane-based micropumps depend upon thermal effects for their operation. An attempt has been made to study the thermal effects in micromechanical structures. One of the thermal-based devices that has been fabricated and successfully used in this research work is the thermally isolated structure described in section 6.5.1 of this

thesis. The direct and indirect experimental temperature values obtained for the device provide a means to validate the proposed model by comparison. Based on this, an attempt is made to develop a model in an analytical approach for the thermally isolated structure. As a first step, a direct approach is explored.

7.3.1 Direct approach

Under steady state conditions, the electrothermal interactions in a semiconductor device in general are based on the following relationships [62].

$$\text{div}[\kappa(T)\ \text{grad}\ T] = -\sigma\ (T)\ (\text{grad}\ \psi)^2 \qquad (7.1)$$

$$\text{div}[\kappa(T)\ \text{grad}\ T] = \rho c\ (\partial T/\partial t) - H \qquad (7.2)$$

where, $\kappa(t)$ represents the thermal conductivity and $\sigma(T)$ is the electrical conductivity. The parameters ρ and c are the specific mass density and specific heat of the material respectively. H is the heat generated locally in the device and ψ is the electric field. The heat flow for the thermally isolated structure under consideration is illustrated in Figure 7.1. From a point where the temperature is maximum, the heat flow occurs along three directions. They are the H_p-through the poly, H_{ox}-laterally through the oxides and H_{amb}-vertically to the ambient. These three components account for heat flow through conduction and convection. The power dissipated through radiation for 170°C, calculated using the equation (6.2), is 4 μW. Hence, the energy loss through radiation can be ignored.

The analytic approach requires certain assumptions to be imposed on the thermally isolated structure under steady state conditions. The resistance of poly is assumed to be independent of temperature and is considered isotropic in its electrical and thermal

conductivities. Geometric nonuniformities are not taken into account. Also, thermal transients are neglected so that $\partial T/\partial t = 0$ in equation (7.2). A constant electric field is assumed along the poly which also implies a uniform current flow throughout its length. An illustration of this approximation is shown in Figure 7.2. It follows from all these assumptions that the poly resistor element acts as the main conductor of heat. This means that the heat flows H_{ox} and H_{amb} in the Figure 7.1 are ignored.

Based on the above assumptions, equation (7.2) reduces to the form

$$d/dx\ [\kappa\ \text{grad}T] = -I^2R/(A\ L) \qquad (7.3)$$

where A and L represent the cross-sectional area and the length of the poly respectively. The current through the poly and the resistance have been denoted by I and R respectively. Equation (7.3) is the basic equation governing the electrothermal interactions of the device under consideration. Solving (7.3), the temperature at any point x along the direction of the poly is given by

$$T(x) = (I^2R/2\kappa AL)\ (Lx - x^2) + T_o \qquad (7.4)$$

where T_o is the ambient temperature. With the poly as the main conductor of heat, boundary conditions are applied to its ends as

$$T(0) = T(L) = T_o = 27°C \qquad (7.5)$$

Now the expected value of the temperature at the centre ($x = L/2$) can be calculated. It is found to be 782°C. Calculation details are provided in Appendix B. The result deviates significantly from the experimentally observed value of 170°C, shown on the thermal map of Figure 6.12. This is undoubtedly the result of not taking into account the heat losses

through the oxide layers of the structure. Before attempting to overcome this discrepancy, a different approach is introduced.

7.3.2 Analogous approach

The basic laws of thermal conduction and temperature difference are analogous to electrical conduction and potential difference [78]. For a one dimensional case the electrical and thermal analogous equivalents are

Voltage ≡ Temperature (T)

Current ≡ Heat in Watts ($W = I^2R$)

Electrical resistance ≡ Thermal resistance (R_t)

One dimensional thermal resistance R_t for a material of length ℓ and cross-sectional area A and thermal conductivity κ is given by the expression [78]

$$R_t = \ell / (kA) \tag{7.6}$$

Hence, the temperature difference ΔT between the two ends of a thermal conductor for a given thermal flow of W can be expressed as

$$\Delta T = [\ \ell / (\kappa A)]\ W \tag{7.7}$$

Using this approach the poly heater element can be modeled and the maximum temperature can be estimated.

7.3.2.1 Two-resistor model

The structure under investigations is modeled as shown in Figure 7.3. Applying the analogy explained above, it can be represented by an electrical equivalent model shown in

Figure 7.4. The poly is represented as two resistors R_1 and R_2 connected in series. V is equivalent to the temperature at the boundaries given by (7.3). The objective is to calculate the unknown temperature V_u at the centre of the node formed by R_1 and R_2. Let the heat introduced at this node be W Watts. An analogy of Kirchoff's current law at this node requires that

$$\Sigma\text{current leaving the node} = \text{Heat introduced.}$$

Applying the law to the model

$$[(V_u - V) / R_1] + [(V_u - V) / R_2] = W \qquad (7.8)$$

Simplifying,

$$V_u - V = \Delta V = W (R_1 R_2) / (R_1 + R_2) \qquad (7.9)$$

Assuming the resistors to be of equal value

$$R_1 = R_2 \qquad (7.10)$$

by analogy, the voltage difference ΔV can be replaced by an equivalent temperature difference ΔT and eqn. (7.9) becomes

$$\Delta T = W R_1/2 \qquad (7.11)$$

Substituting for various values, (shown in Appendix B), the unknown temperature has been found to be 782°C. The calculated figure is the same as the value obtained using the direct approach but still not with the experimental value. As pointed out earlier, the model has to be refined further to incorporate the heat lost through the oxide layers of the structure. Therefore, an attempt has been made to develop a model by considering a more

realistic description of the thermally isolated structure.

7.3.2.2 Four-resistor model

This model is based on the heat flow configuration along the poly and the oxide (H_p and H_{ox}) in the absence of gas flow. In general due to large thermal resistance, air can assumed to be an insulator in the absence of gas flow. The thermal conductivity of oxide is 0.011W/cm °C while the thermal conductivity of air is 0.0024 W/cm °C. Hence, the heat lost through the air (H_{amb}) can be neglected. Therefore, it is assumed in the analysis that the heat flow takes place only laterally. Using the analogous approach a two dimensional model can be formulated.

The analogous electrical model for this situation is shown in Figure 7.5. The model includes two additional resistors compared to the two resistor model, each of value R_2 for the oxide layers. The four end voltages all correspond to the boundary temperature conditions. The heat generated, W, at the centre node (where temperature is to be calculated) is due to the poly resistor. Applying the Kirchoff's law in the same manner as that of the two resistor model, the temperature at the centre node can be derived to be

$$\Delta T = (W R_1 R_2) / [2 (R_1 + R_2)] \qquad (7.12)$$

The temperature at the centre is calculated to be 174°C. This figure matches well with the experimentally obtained value of 170°C, shown in Figure 6.12.

The above-mentioned modeling scheme gives the temperature distribution along the polysilicon with the maximum temperature located symmetrically at the center. However, we notice that there is a shift in the maximum temperature value from the centre of the structure. There could be many reasons for this shift. Due to unavailability of information about the process parameters from the CMOS foundry, it is very difficult to determine the

exact cause for this temperature shift. However, several possible reasons can be suggested and are indicated in Figure 7.6. Figure 7.6 (a) illustrates a local structural defect in the poly which could cause the hot spot to move to that location. Figure 7.6 (b) shows the possibility of a gradual thinning of poly due to processing conditions which could also cause the shift in the location of the maximum temperature. Figure 7.6 (c) points out a possible defect in the oxide which could similarly shift the location of the maximum temperature.

If we can initiate detailed information exchange with the CMOS foundry in the future, it will be possible to develop better thermal models to analyse these micromechanical devices.

7.4 Limitations of the analytical models

Although the analytical approach using the analogous model gives satisfactory results, it should be noted that the approach is valid for the specific structure and conditions. Incorporation of the variation of mechanical and electrical parameters becomes very difficult and sometimes impossible with analytical models. For a realistic simulation, numerical modeling approaches become necessary so that a more meaningful study can be carried out [72].

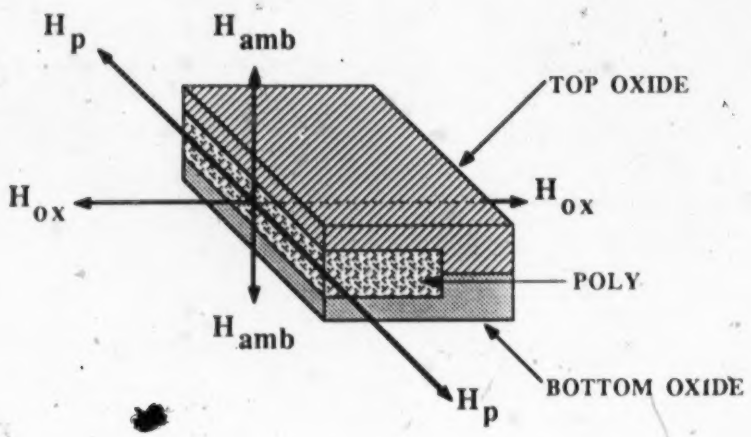


Figure 7.1. Illustration of various heat flows from the polysilicon heater element.

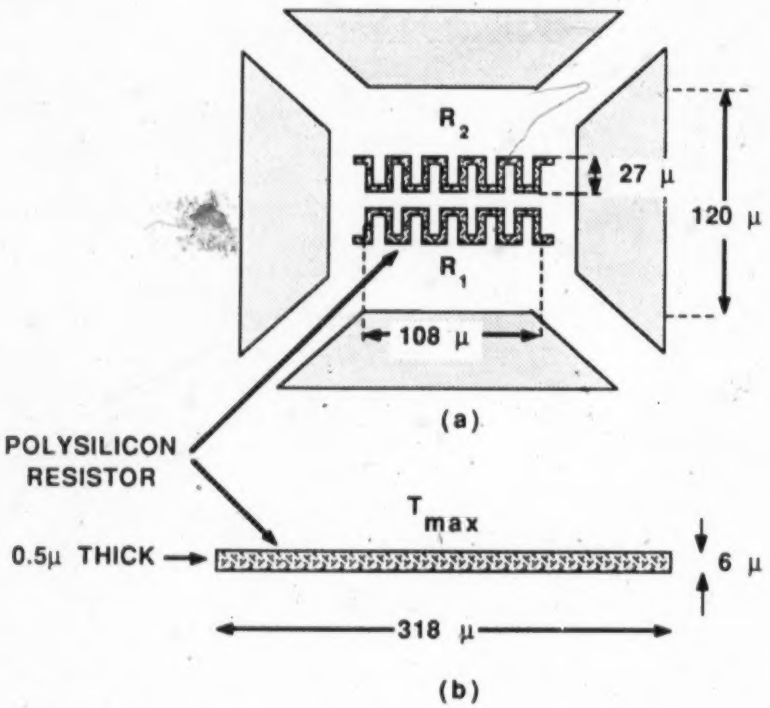


Figure 7.2. Thermally isolated structure considered for modeling.

(a) Complete structure (b) Approximated structure used for modeling.

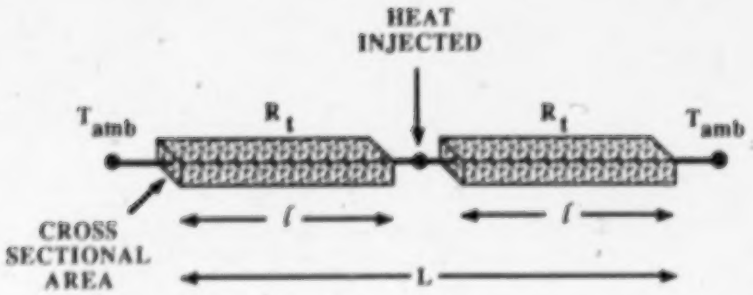


Figure 7.3. Structural equivalent of the two resistor model.

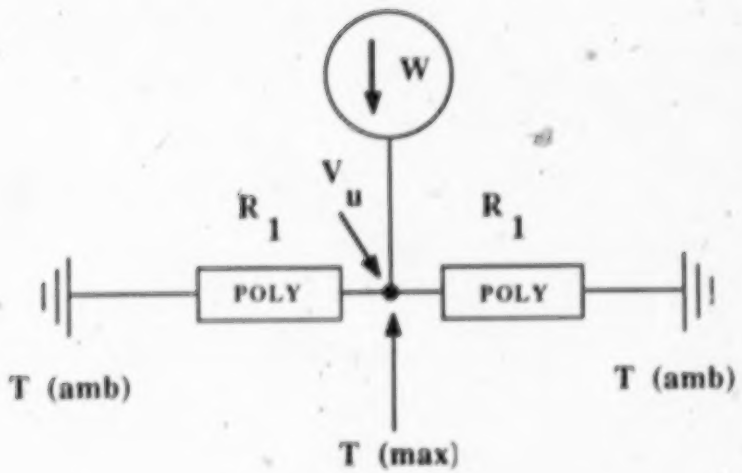


Figure 7.4. Two resistor model.

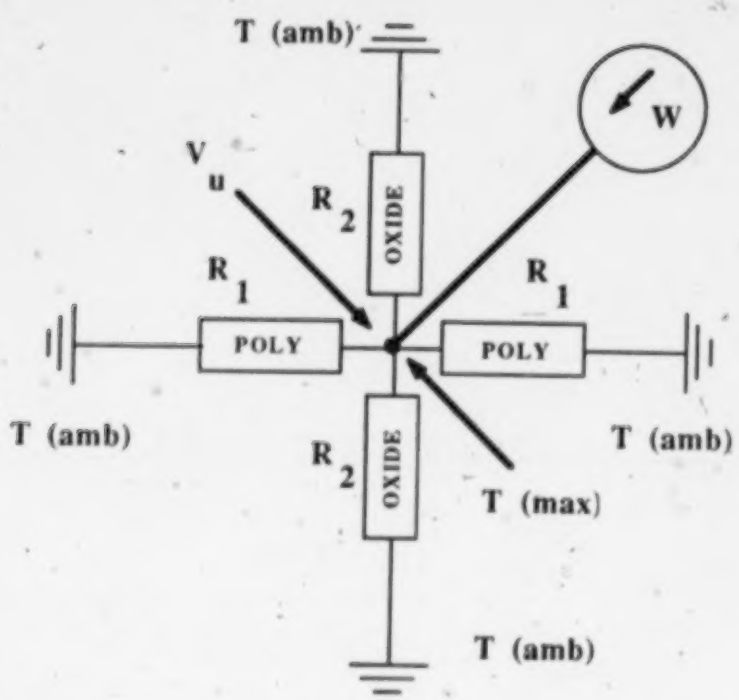


Figure 7.5. Four resistor model.

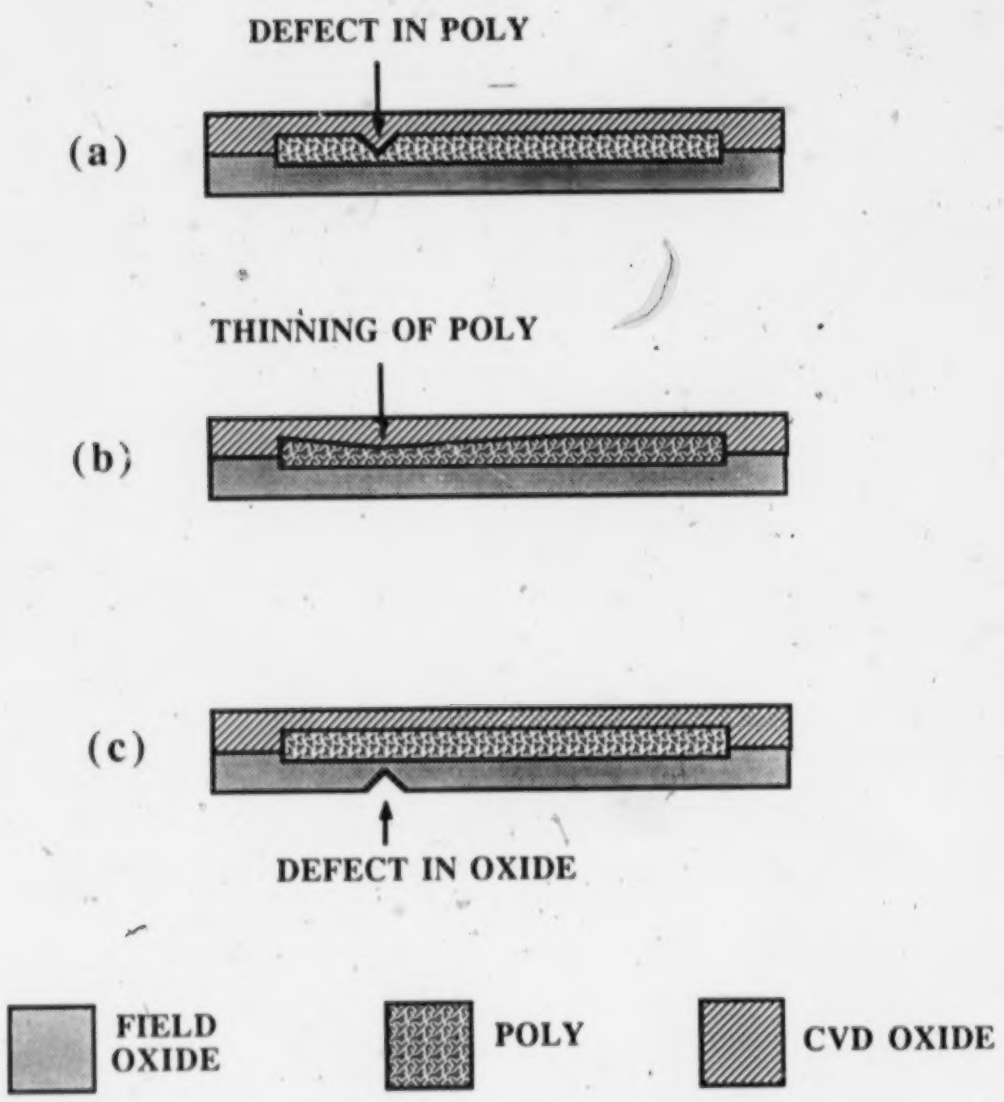


Figure 7.6. Illustration of structural parameter variation

(a) Local defect in poly, (b) thickness variation in poly and (c) local defect in oxide.

8. CONCLUSION

The major aim of this work is to develop simple, economical and efficient schemes for the fabrication of sensors and actuators. The purpose behind this aim is to realize the possibility of fabricating sensors and actuators in an inexpensive manner. Interestingly enough, many important technological developments also become feasible by this process. A link has been established between the IC and sensor technologies. The link has given rise to many useful features that fulfill some of the important needs of today's sensor technology. This chapter summarizes the approach, its significant aspects and the resulting contributions of this research.

8.1 Summary of contributions

From a careful investigative study on a CMOS IC fabrication process, it was discovered that the process sequence was not influenced in any way by the layout information. This discovery provided the basis to establish a link between the IC and sensor technology. Consequently, a scheme has been developed whereby most of the fundamental building blocks for the fabrication of sensors and actuators can be obtained simply by providing appropriate layout information to the CMOS foundry. The scheme which integrates the sensor fabrication with the IC technology consists of two parts, namely the layout design and the post-processing. The layout design aspect allows the user to generate layout information that would form the basic building blocks for the sensor as well as the circuits for the on-chip electronics. This layout design method is derived from the standard layout layers supplied by the foundry. The post-processing aspect is the process which converts the basic structure formed on the CMOS chip into a sensor or actuator, without affecting the active components formed on the chip. The important and significant consequences of this approach are summarised below:

- Sensor and actuator fabrication becomes feasible in any laboratory with moderate equipment facilities.

- The customized approach of sensor fabrication has been replaced by a regularized approach. The regularized approach implies that the fabrication steps remain fixed for different devices unlike the customized approach where the fabrication steps need to be altered depending on the device fabricated.

- The sensor fabrication process does not require any process modifications by the CMOS foundry.

- Integration of on-chip electronics becomes easily feasible. This useful feature comes through the fact that the sensor fabrication process does not alter in any way the circuit forming capabilities of the CMOS process. This feature is important for the development of 'smart' sensors with many capabilities.

Several sensors and actuators were designed, fabricated and tested in order to verify the sensor and actuator fabrication process. Initially, humidity sensor elements were fabricated [81] and later developed into an integrated system by incorporating on-chip electronics for signal conversion [82]. The subsequent efforts centered upon silicon micromachining, a field of growing interest in sensor technology. It was found that the incorporation of silicon micromachining techniques as the post-processing step in the regularized scheme led to the formation of several micromechanical structures. Using this technique, polysilicon microbridges [83, 84], sandwiched oxide microbridges, cantilevers and suspended plates were successfully fabricated [85-87]. With CMOS polysilicon as resistor and heater elements several functional devices were realised and tested [88, 89]. Fabrication of micromechanical structures using the SACMOS process was attempted and successful results obtained [7]. This demonstrates the issue of portability between commercial processes. Micromechanical devices such as thermal resolution test targets and accelerometers on a CMOS chip have been fabricated and are currently being characterized.

The success in the stages of fabrication and testing has prompted many research groups towards obtaining insights into the functioning of the CMOS micromechanical devices and their characterization. It includes modeling of mechanical and thermal effects in microstructures. As part of this thesis, an analytical model has been developed to analyse the thermally isolated micromechanical device. The results are compared with the experimental findings. Wherever possible, analytical results have been obtained for devices and compared against the experimental data. Significant findings or conclusions have not been possible at this stage on these comparative studies.

8.2. Limitations and outlook

The use of commercial IC processes for sensor fabrication has significant merits and potential but in its present form has two limitations. The choice of commercial CMOS technology for sensor fabrication imposes certain limitations on the approach. First, the available process-layers become restricted for the designers. For example, silicon nitride is a useful process-layer that could be used for silicon micromachining and micromechanical structures [15]. This process-layer is not supported by the CMOS process offered by Northern Telecom [44]. Hence, sensors or actuators requiring this process-layer cannot be realized using this CMOS process. A significant example of this limitation includes the most popular micromechanical pressure sensor. The device makes use of a thin closed silicon diapharagm as the pressure-sensitive element. The silicon diapharagm is fabricated using electrochemical etching techniques performed from the back of the silicon wafer [38]. To facilitate the etching, it is essential for the sillicon wafer to have an epitaxial layer. Since commercial CMOS processes do not have an epitaxial layer, using the approach reported in this thesis, performing electrochemical etching and realizing the closed diaphragm become difficult.

Secondly, the vertical dimensions (thicknesses) of the various process-layers are specified by the CMOS foundry. This leaves the designer with a limited choice of device

dimensions, particularly the thickness. In fabricating micromechanical structures, thickness of the structural material is a significant parameter since it determines the mechanical properties of the micromechanical device. Subsequent micromechanical and thermal modeling is also hindered by this restriction.

The two above-mentioned limitations are imposed by the chosen CMOS process and not by the approach detailed in this thesis. There are numerous commercial IC processes available such as BICMOS, bipolar, analog and digital gate arrays. Each of these IC processes has its own process-layers to offer. So it is up to the user to choose the appropriate IC technology and adapt the requlatized approach to fabricate the type of sensor or actuator of interest. To overcome the selection of process-layer limitation, the regularized approach could be extended to the other widely used commercial IC technologies listed above. By using BICMOS and bipolar IC processes, the user gets a different selection of process-layers for sensor design compared to the CMOS process. Further, it will allow the possibility of accommodating electrochemical etching as the post-processing step, enabling the production of many useful sensors and actuators.

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APPENDIX A

SPICE program listing and the simulated ouput of the oscillator.

```
1********07/23/87 ********  SPICE 2G.6   3/15/83 *********20:17:59******
0*   SIMULATION OF OSCILLATOR
0****    INPUT LISTING.              TEMPERATURE =   27.000 DEG C
0******************************************************************************
*
.WIDTH IN=80 OUT=80
*
.OPTIONS NOMOD ABSTOL=1N VNTOL=1U CPTIME=500 NUMDGT=4 LIMPTS=1000
*
.MODEL NTNMOS NMOS(LEVEL=2 VTO=0.9 PB=0.7
+ KP=30E-6     GAMMA=1.3    PHI=0.7      LAMBDA=0.01
+ CGSO=4.0E-10  CGDO=4.0E-10  CGBO=2.0E-10  RSH=15.0
+ CJ=4.0E-4     MJ=2.0       CJSW=8.0E-10  MJSW=2.0
+ JS=1.0E-6     TOX=8.5E-8    NSUB=1.0E16   XJ=1.0E-6
+ LD=0.7E-6     UO=750       VMAX=5.0E4    UCRIT=5.0E4
+ UEXP=0.14)
*
.OPTIONS NOMOD ABSTOL=1N VNTOL=1U CPTIME=500 NUMDGT=4
.MODEL NTPMOS PMOS(LEVEL=2 VTO=-0.9 PB=0.7
+ KP=9.5E-6     GAMMA=0.6    PHI=0.6      LAMBDA=0.03
+ CGSO=4.0E-10  CGDO=4.0E-10  CGBO=2.0E-10  RSH=75.0
+ CJ=1.8E-4     MJ=2.0       CJSW=6.0E-10  MJSW=2.0
+ JS=1.0E-6     TOX=8.5E-8    NSUB=2.0E15   XJ=0.9E-6
+ LD=0.6E-6     UO=250       VMAX=3.0E4    UCRIT=1.0E4
+ UEXP=0.03)
*
*  CIRCUIT DESCRIPTION:
*
R1 2 0 850K
MB1 2 2 1 1 NTPMOS  W=42U L=14U AD=210P AS=210P
MB2 3 2 1 1 NTPMOS  W=42U L=14U AD=210P AS=210P
MB3 4 5 0 0 NTNMOS  W=28U L=14U AD=140P AS=140P
```

```
MB4 5 5 0 0 NTNMOS  W=28U L=14U AD=140P AS=140P
MB5 3 3 4 4 NTNMOS  W=14U L=28U AD=70P AS=70P
MB6 6 3 5 5 NTNMOS  W=14U L=28U AD=70P AS=70P
MB7 6 6 1 1 NTPMOS  W=42U L=14U AD=210P AS=210P
MB8 7 6 1 1 NTPMOS  W=42U L=14U AD=210P AS=210P
MB9 10 5 0 0 NTNMOS W=28U L=14U AD=140P AS=140P
*
MK1 7 8 9 9 NTNMOS W=28U L=14U AD=140P AS=140P
MK2 10 8 9 1 NTPMOS W=56U L=14U AD=250P AS=250P
*
MS1 11 9  1 1 NTPMOS  W=42U L=14U AD=210P AS=210P
MS2 8  9 11 1 NTPMOS  W=63U L=14U AD=300P AS=300P
MS3 0  8 11 1 NTPMOS  W=63U L=14U AD=300P AS=300P
MS4 8  9 12 0 NTNMOS  W=42U L=14U AD=210P AS=210P
MS5 12 9  0 0 NTNMOS  W=28U L=14U AD=140P AS=140P
MS6 1  8 12 0 NTNMOS  W=42U L=14U AD=210P AS=210P
CS 9 0 30PF IC=0
*
CO 8 0 15PF IC=0
*
*  VOLTAGES:
*
VDD 1 0 DC 10
*
*
*
.OP
.TRAN 2US 50US UIC
.PLOT TRAN V(9) V(8)
*
.END
```

1********07/23/87 ***** SPICE 2G.6 3/15/83 *********20:17:59******

0* SIMULATION OF OSCILLATOR

0**** SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C

0**********

NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE

(1) 10.0000 (2) 8.2264 (3) 4.0118 (4) 1.5843

(5) 1.6234 (6) 8.1514 (7) 10.0000 (8) 6.0584

(9) 5.1967 (10) 0.0000 (11) 8.5400 (12) 1.8517

VOLTAGE SOURCE CURRENTS

NAME CURRENT

VDD -3.756d-04

TOTAL POWER DISSIPATION 3.76d-03 WATTS

1********07/23/87 ********* SPICE 2G.6 3/15/83 *********20:17:59******

0* SIMULATION OF OSCILLATOR

0**** OPERATING POINT INFORMATION TEMPERATURE = 27.000 DEG C

0**********

0**** MOSFETS

0	MB1	MB2	MB3	MB4	MB5	MB6	MB7
0MODEL	NTPMOS	NTPMOS	NTNMOS	NTNMOS	NTNMOS	NTNMOS	NTPMOS
ID	-9.68e-06	-1.14e-05	1.14e-05	1.14e-05	1.14e-05	1.14e-05	-1.14e-05
VGS	-1.774	-1.774	1.623	1.623	2.428	2.388	-1.849
VDS	-1.774	-5.988	1.584	1.623	2.428	6.528	-1.849
VBS	0.000	0.000	0.000	0.000	0.000	0.000	0.000
VTH	-0.876	-0.869	0.869	0.869	0.884	0.880	-0.876
VDSAT	-0.676	-0.684	0.441	0.441	0.936	0.916	-0.733
GM	2.16e-05	2.52e-05	3.07e-05	3.07e-05	1.41e-05	1.44e-05	2.34e-05
GDS	3.72e-07	4.54e-07	2.37e-07	2.36e-07	1.43e-07	1.37e-07	4.32e-07
GMB	6.17e-06	7.11e-06	1.99e-05	1.99e-05	8.25e-06	8.46e-06	6.61e-06
CBD	3.03e-15	4.14e-16	5.26e-15	5.08e-15	1.40e-15	2.63e-16	2.85e-15
CBS	3.77e-14	3.77e-14	5.60e-14	5.60e-14	2.80e-14	2.80e-14	3.77e-14
CGSOVL	1.68e-14	1.68e-14	1.12e-14	1.12e-14	5.60e-15	5.60e-15	1.68e-14
CGDOVL	1.68e-14	1.68e-14	1.12e-14	1.12e-14	5.60e-15	5.60e-15	1.68e-14
CGBOVL	2.56e-15	2.56e-15	2.52e-15	2.52e-15	5.32e-15	5.32e-15	2.56e-15

CGS	1.46e-13	1.46e-13	9.56e-14	9.56e-14	1.01e-13	1.01e-13	1.46e-13
CGD	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
CGB	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00

0	MB8	MB9	MK1	MK2	MS1	MS2	MS3
0MODEL	NTPMOS	NTNMOS	NTNMOS	NTPMOS	NTPMOS	NTPMOS	NTPMOS
ID	4.82e-12	-1.38e-11	1.20e-11	-9.67e-14	-1.29e-04	-8.91e-05	-4.02e-05
VGS	-1.849	1.623	0.862	0.862	-4.803	-3.343	-2.482
VDS	0.000	0.000	4.803	-5.197	-1.460	-2.482	-8.540
VBS	0.000	0.000	0.000	4.803	0.000	1.460	1.460
VTH	-0.882	0.877	0.861	-1.689	-0.880	-1.235	-1.221
VDSAT	-0.727	0.435	0.000	0.000	-2.920	-1.706	-1.038
GM	4.84e-12	1.84e-11	3.10e-08	0.00e+00	4.22e-05	8.38e-05	6.32e-05
GDS	2.89e-05	4.98e-05	6.26e-11	0.00e+00	6.73e-05	3.16e-06	1.73e-06
GMB	7.32e-12	5.58e-11	2.29e-08	0.00e+00	1.02e-05	1.29e-05	1.03e-05
CBD	3.78e-14	5.60e-14	9.06e-16	1.93e-16	4.01e-15	1.23e-15	2.31e-16
CBS	3.78e-14	5.60e-14	5.60e-14	7.28e-16	3.68e-14	5.64e-15	5.66e-15
CGSOVL	1.68e-14	1.12e-14	1.12e-14	2.24e-14	1.68e-14	2.52e-14	2.52e-14
CGDOVL	1.68e-14	1.12e-14	1.12e-14	2.24e-14	1.68e-14	2.52e-14	2.52e-14
CGBOVL	2.56e-15	2.52e-15	2.52e-15	2.56e-15	2.56e-15	2.56e-15	2.56e-15
CGS	1.09e-13	7.17e-14	9.56e-14	0.00e+00	1.29e-13	2.18e-13	2.18e-13
CGD	1.09e-13	7.17e-14	0.00e+00	0.00e+00	8.13e-14	0.00e+00	0.00e+00
CGB	0.00e+00	0.00e+00	0.00e+00	2.91e-13	0.00e+00	0.00e+00	0.00e+00

0	MS4	MS5	MS6
0MODEL	NTNMOS	NTNMOS	NTNMOS
ID	8.91e-05	3.03e-04	2.14e-04
VGS	3.345	5.197	4.207
VDS	4.207	1.852	8.148
VBS	-1.852	0.000	-1.852
VTH	1.794	0.872	1.784
VDSAT	1.069	2.513	1.634
GM	1.87e-04	9.57e-05	1.65e-04
GDS	1.33e-06	9.08e-05	2.79e-06
GMB	3.64e-05	4.57e-05	5.29e-05

CBD	9.01e-16	4.23e-15	3.60e-16
CBS	6.31e-15	5.53e-14	6.30e-15
CGSOVL	1.68e-14	1.12e-14	1.68e-14
CGDOVL	1.68e-14	1.12e-14	1.68e-14
CGBOVL	2.52e-15	2.52e-15	2.52e-15
CGS	1.43e-13	9.13e-14	1.43e-13
CGD	0.00e+00	3.60e-14	0.00e+00
CGB	0.00e+00	0.00e+00	0.00e+00

```
1********07/23/87 ******** SPICE 2G.6  3/15/83 *********20:17:59******
0*  SIMULATION OF OSCILLATOR
0****    TRANSIENT ANALYSIS          TEMPERATURE =  27.000 DEG C
0******************************************************************************

0LEGEND:

*: V(9)
+: V(8)
X
   TIME     V(9)

(*)---------- 0.000d+00    2.000d+00    4.000d+00
              ------------------------------

(+)---------- -5.000d+00   0.000d+00    5.000d+00
              ------------------------------
0.000d+00  1.284d-01 .*       .+          .          .          .
2.000d-06  1.238d+00 .     *  .           .          +          .
4.000d-06  2.175d+00 .        .*          .          +          .
6.000d-06  3.077d+00 .        .     *     .          +          .
8.000d-06  3.947d+00 .        .           *          +          .
1.000d-05  4.788d+00 .        .           .     *    +          .
1.200d-05  5.601d+00 .        .           .          *+         .
1.400d-05  6.384d+00 .        .           .          +.    *    .
1.600d-05  6.154d+00 .        +           .          .*         .
1.800d-05  5.377d+00 .        +           .          *.         .
2.000d-05  4.609d+00 .        +           .     *    .          .
2.200d-05  3.850d+00 .        +           *          .          .
2.400d-05  3.220d+00 .        .+          *          .          .
2.600d-05  3.538d+00 .        .           *          .+         .
2.800d-05  4.402d+00 .        .           .     *    +          .
3.000d-05  5.228d+00 .        .           .          *+         .
3.200d-05  6.029d+00 .        .           .          X          .
3.400d-05  6.697d+00 .        .           .     +    .     *    .
3.600d-05  5.809d+00 .        +           .          .*         .
3.800d-05  5.035d+00 .        +           .     *    .          .
4.000d-05  4.272d+00 .        +           .     *    .          .
4.200d-05  3.522d+00 .        +           *          .          .
4.400d-05  3.133d+00 .        .     X     .          .          .
4.600d-05  4.067d+00 .        .           *          +          .
4.800d-05  4.904d+00 .        .           .     *    +          .
5.000d-05  5.715d+00 .        .           .          *+         .
              ------------------------------

Y
0
     JOB CONCLUDED
0    TOTAL JOB TIME       136.77
```

APPENDIX B

Derivation of heat density

The general heat flow equation [62] in any electrical device is expressed as

$$\text{div}[\kappa(T)\ \text{grad}\ T] = -\sigma(T)\ (\text{grad}\psi)^2 \qquad \text{(B.1)}$$

Under steady state conditions assumed in section 7.2.1 the right hand side can be approximated as

$$-\sigma\ (V/L)^2 \qquad \text{(B.2)}$$

where, V/L is the electric field.

(B.2) can be written as

$$-(L/RA)(V/L)^2 \qquad \text{(B.3)}$$

where, R is the electrical resistance and A is the effective cross-sectional area. This can be rewritten as

$$-I^2R/AL \qquad \text{(B.4)}$$

(B.4) represents the heat density and (B.1) can be written as

$$\text{div}[\kappa(T)\ \text{grad}\ T] = -I^2R/AL. \qquad \text{(B.5)}$$

Derivation of temperature

Starting from eqn. (7.4)

$$d/dx[\kappa\ \text{grad}\ T] = -I^2R/AL \qquad \text{(B.6)}$$

This can be rewritten as

$$d/dx\ dT/dx = (1/\kappa)(-I^2R/AL)$$

$$T = -(1/\kappa)(I^2R/A.L) \iint dx\ dx$$

$$T = -(1/\kappa)(I^2R/A.L)\ [(x^2/2) + bx + c] \qquad \text{(B.7)}$$

Substituting the boundary conditions

at $x = 0$, $T = 27°C$

$$\therefore c = (-27)/(I^2R/A.L)$$

at x = L, T = 27°C

$$\therefore b = -L/2$$

Hence, (B.7) can be written as

$$T = (1/2\kappa)(I^2R/A.L)[Lx - (x^2/2)] + 27 \qquad (B.8)$$

The highest temperature will occur at the centre of the poly strip (x = L/2) and calculating this temperature

$$T(max) = (I^2R/8\kappa A)L + 27 \qquad (B.9)$$

Substituting the values $I^2 R = 8.55$ mW, $\kappa = 1.5$W/cm °C, L = 318μm and

$A = 3\ \mu m^2$

$$T(max) = 782°C \qquad (B.10)$$

Analogous approach - Two resistor model

The thermal resistance [78] is defined by the expression

$$R_t = \ell / (\kappa A) \qquad (B.11)$$

Since the two resistor model divides the poly resistor into two halves the R_t of each element can be expressed as

$$R_t = \ell / (2\kappa A) \qquad (B.12)$$

Since the length ℓ is L/2 (B.12) becomes

$$R_t = L / (4\kappa A) \qquad (B.13)$$

Computing the maximum temperature using the values $I^2 R = W = 8.55$ mW, $\kappa = 1.5$W/cm °C, L = 318 μm and $A = 3\ \mu m^2$

$$\Delta T = (W R_t) / 2 \text{ and } T(max) = \Delta T + 27°C$$

$$\therefore T(max) = 782°C$$

Four resistor model

In the four resistor model

$$R_1 = R_{t\,(poly)} = L_{poly} / (4\kappa_{poly} A_{poly}) \qquad (B.14)$$

$$R_2 = R_{t\,(ox)} = L_{ox} / (4\kappa_{ox} A_{ox}) \qquad (B.15)$$

Computing the maximum temperature using the values $I^2 R = W = 8.55$ mW, $\kappa_{poly} = 1.5$W/cm °C, $L_{poly} = 318\mu$m, $A_{poly} = 3\ \mu m^2$, $\kappa_{ox} = 0.011$W/cm °C, $L_{ox} = 60\ \mu$m and $A_{ox} = 6.36\ \mu m^2$

$$\Delta T = (W R_1 R_2) / [2(R_1 + R_2)] \text{ and } T(max) = \Delta T + 27°C$$

$$\therefore T(max) = 174°C$$

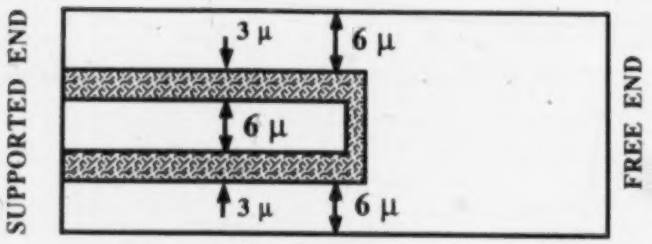
Analysis of cantilever microactuator

Figure B.1 shows the top and cross-sectional view of the cantilever structure. Computing the equivalent thermal resistance for the poly and the oxide, an analogous four resistor model as described in the previous section can be derived and the temperature rise ΔT can be calculated.

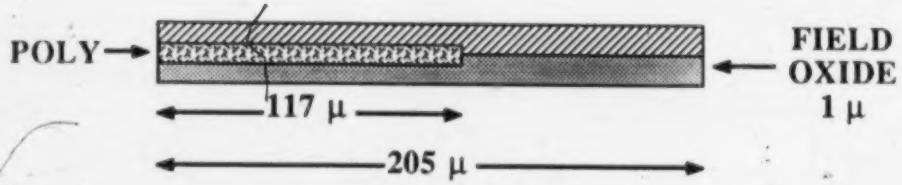
Computing the maximum temperature using the values $I^2 R = W = 5.6$ mW, $\kappa_{poly} = 1.5$W/cm °C, $L_{poly} = 234\ \mu$m, $A_{poly} = 3\ \mu m^2$, $\kappa_{ox} = 0.011$W/cm °C, $L_{ox} = 6\ \mu$m and $A_{ox} = 234\ \mu m^2$

$$\Delta T = (W R_1 R_2) / [2(R_1 + R_2)]$$

$$\Delta T = 31°C.$$



(a)



(b)

Figure B.1. Structural details of the cantilever microactuator.

(a) Top view and (b) cross-sectional view.